# Fabrication of Scintillation Counters and testing techniques using Cosmic Ray Setup and Data Acquisition

## Technical Note

***On***

***Lab Activities of High Energy Physics Group at Panjab University, Chandigarh***


***Written, composed and compiled***

***by***

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# PREFACE

This “Technical Note” is intended to serve as guide for the research students working in the field of Experimental High Energy Physics (EHEP). The description on various aspects is a outgrowth of a high-tech laboratory being established by EHEP group in the department of Physics Panjab University Chandigarh for fabricating and testing various detector parts for the two major experiments namely D-Zero experiment at Fermilab U.S.A and CMS experiment at CERN. The task for establishing a high tech laboratory included planning various experiments, learning relevant techniques, setting up of measuring and calibration apparatus, data-taking and analysis, as well as procurement of materials for fabrication of detector parts. The author of this write-up had been an active participant for establishing the high energy physics laboratory as well as fabrication of scintillation tiles of hadron outer calorimeter for CMS experiment at CERN. Since setting up of the EHEP laboratory involved variety of technical procedures and sophistications, the need was felt, of providing descriptions in the shape of this ‘Technical Note’. The description on various aspects gives ready reference for all those who have decided an entry into experimental high energy physics group in the department. It is an appropriate support material for researchers and students.

This ‘technical Note’ is divided into five chapters. Chapter one is an introductory chapter which gives the general idea of detector fabrication in lab. Chapter two describes the fabrication aspects of the scintillator detectors and counters using plastic scintillator, light guides and photomultipliers. The information contained in this chapter provides the reader a practical guide to fabricate a scintillator detector and know about various components used. A simple technique to test the detector with the help of an oscilloscope is also described in this chapter.

Chapter 3 describes the cosmic ray set up and the electronics set up for signal formation, its processing and the data acquisition. In our setup, we have used standard NIM and CAMAC systems which are commercially available. Functional description of the used modules and their application to our experiment is given in this chapter. The selected modules can perform various operations on the originated pulse signals from the detectors. For performing various experiments, co-axial cables with lemo connectors are used to transmit signals from one module to the other. Block diagrams are used to explain various experiments which can be performed using this set up.

Chapter 4 gives the details of the fabricated detector part for the CMS experiment at CERN. These detector parts are known as scintillation tiles for the outer hadron calorimeter in CMS detector. These tiles were successfully fabricated and tested in the department and finally installed in the main detector at CERN. A computer controlled Fiber Scanner Machine was designed developed and fabricated in the department for testing attenuation of the fibers used for the scintillation tiles. Complete details of this machine are also given in chapter 4.

Chapter 5 handles the basics of Electricity and Electronics in general which are assumed to be understood before handling the set up using electronics and electrical gadgets throughout.

The detailed description of various electronic modules and other materials, provided by the manufacturers, is attached with this 'Technical Note' in annexure in the end.

The author has made liberal use of the materials available in the works of eminent authors in preparing this 'Technical Note'. He has tried to fashion the vast amount of material available into coherent body of description.

I am grateful to our faculty members Prof J.M.Kohli, Prof Suman Beri, Prof J.B.Singh and Prof Manjit Kaur with whom I had been associated with, during fabrication of detector parts as well as establishing the sophisticated data acquisition lab in the department. It is all their motivated encouragement that I could compile some details in the shape of this 'Technical Note'.

Towards the preparation of lab experiments and fabrication of detector parts for CMS experiment, the untiring efforts of the technical group members Mr. Joginder Pall, Mr. V.B.Tiwari, Mr. D.L.Arora, Mr. Tej Paul Singh, Mr. Rachpall Singh are acknowledged with gratitude. However on this account special thanks are due to Mr. Baljinder Singh and Dr. Vipin Bhatnagar for their full technical support.

I thank research scholars, Ashok Kumar, Harinder Singh, and Research Associate Dr. Rajwant Kaur and Dr. Nitesh Soni for the fruitful discussions during the experimental setup in the lab for both D-Zero and CMS experiment.

I also thank Mr Sanjeev Gautam in giving useful help in compiling the manuscript and bringing out this 'Technical Note' in presentable form and quality.

Finally, I would like to thank my parents, in particular my respected father Sh. Rameshwar Dass Bhandari for all their blessings and encouragement which led me write and compile this 'Technical Note'.

I shall feel highly satisfied if this produced material meets requirements of the researchers and students for whom it is written. Suggestions for improvement, additions or subtraction of any topic and also corrections to the written material are welcomed and shall be highly appreciated.

V.K.Bhandari

# Fabrication of Scintillation Counters and testing techniques using Cosmic Ray Setup and Data Acquisition

## Contents

# Experimental High Energy Physics Group (EHEP)
# at
# Panjab University Chandigarh

Since early 1960 Experimental High Energy Physics (EHEP, http://www.puhep.res.in) Group has been involved in various experiments based on cosmic rays as well as interactions of beam particles from accelerators. From the year 1990 onwards the group has been working in major experiments namely, Collider Beam Experiments and Relativistic Heavy Ions Interactions. The group members have actively participated and contributed considerably in making new discoveries like "The Discovery of Top Quark" and experimental evidence of "Quark Gluon Plasma" and CP violation in $B\overline{B}$ system etc. At present the group is actively participating in various collaborations for study and discovery of fundamental basic smallest particles which constitute matter and evolution of universe. These frontline experiments are: CMS experiment (CERN), DZERO experiment (Fermilab U.S.A.), LEP2 experiment (CERN), BELLE experiment (KEK Japan), STAR experiment (RHIC) and ALICE (CERN).

The High Energy experimental group has well established research lab for performing various experiments connected with Collider Physics at CERN and Fermilab. The infrastructure includes the cosmic ray set-up, fast electronics set-up and computational facilities. The lab is further equipped for the fabrication of various detector parts like scintillation counters. The electronics set-up consists of NIM and CAMAC systems having various independent modules like Discriminators, Logic Units, Fan-In Fan-Out, Scalars, Analog to Digital Converters. Time to Digital Converters and High Voltage Power Supply Units. The whole setup is interfaced to the dedicated computer for data storage of various experiments performed for the testing of the fabricated parts of the detector. A completely self developed Fiber Scanning Machine is also available for testing the attenuation of the optical fibers to be used for fabrication of the detector parts to be finally installed at CERN. The lab is further equipped with the test and measuring units like oscilloscope, multi-meters, variable power supplies, IC tester and various electronic components needed for developing any type of system needed from time to time. The installed equipments in the lab can any time be modified for performing any new experiment during the research activities. A Probe Station for probing the silicone vertex detectors has recently been installed in the lab for testing the silicon detectors.

EHEP Group has a well established sophisticated computer lab with 1 mbps lease line internet facility and a cluster of ten CPU's, 400GB storage space and 12 PC nodes. The computer lab is equipped with a 48 hour back uninterrupted power supply (UPS) (1+1). The group is further in the process of installing ten more CPU's, 1 TB storage space for the grid computing project. The computer lab has also the video conferencing facility on lease line with Fermilab and CERN. The lab has its own web server and email server (http://www.puhep.res.in)

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# COSMIC RAY SETUP & DATA ACQUISITION AT PANJAB UNIVERSITY CHANDIGARH

**Photo 1: Overall View of setup at CMS/D-Zero Lab**

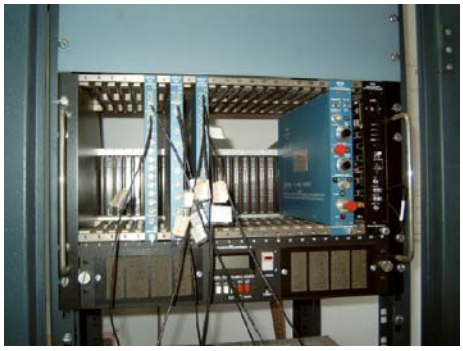


**Photo 2: Camac Crate**

**Photo 3: Camac Crate**

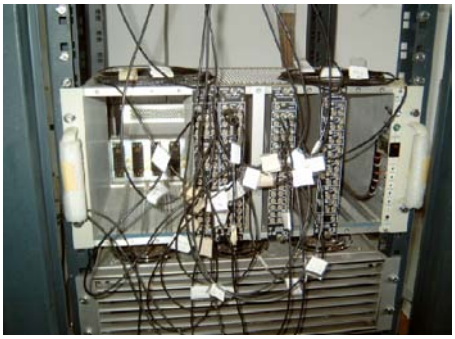


**Photo 4: NIM BIN**

**Photo 5: NIM BIN**

**Photo 6: Overall View of the Data Acquisition Setup**

**Photo 7: HV Power Supply**

**Photo 8: The detector setup**

**Photo 9: PC Attached to DAQ**

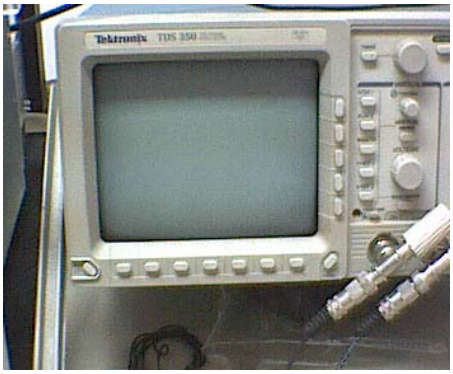



**Photo 10: CRO used in the setup**

**Photo 11 & 12: Assembled Detectors to be used as peddles**

**Photo 13 Mounted Detector as peddle** **Photo 14 Mounted tile as Counter**

## *CHAPTER 1:*

## *INTRODUCTION:*

The Scintillation detector is a detector device most often used in nuclear and particle physics today. Scintillator is certain material which when struck by particle or radiation emit a small flash of light called scintillation. Scintillator material produces a pulse of light shortly after the passage of particle. These scintillations can be converted in electrical pulses by coupling to an amplifying device such as a photo multiplier. These pulses can be analyzed and counted electronically to give information concerning the incident radiation.

The aim of this write up is to make oneself familiar with the techniques for testing and calibrating a charged particle using cosmic ray muons. The cosmic ray setup consists of coincidence of three detectors and the electronics for the determination of coincidences. (See figure 1.1 for block diagrame). As is clear from the block diagram, you can test your charged particle detector with relativistic charged particles using cosmic ray muons as trigger. Muons are formed from the decay of pions, which are created in the upper atmosphere by incident ray protons. Because the muons are more penetrating, they manage to reach the surface of the earth without being absorbed they eventually stop in matter and decay. We shall be learning the techniques involved

(i) in fabricating the detector
(ii) in setting up a coincidence for cosmic ray muons
(iii) in analyzing signals of independent detectors as well as signals obtained from coincidences

The available "COSMIC RAY SET UP AND DATA ACQUISITION" provides an opportunity to learn about several components that are necessary to setup any experiment in High Energy Physics. The electrical signals from the detector provide variety of information which need to be processed by an electronic system. We need to have a setup with which help we are able to perform various tasks like sorting out various signals from the detector, get energy information, determine the timing between the two signals etc. This information allow us to decide about the event taking place by recording it in some recording device. In our data acquisition setup we are using NIM and CAMAC standards. Various NIM and CAMAC modules in use of our setup are discriminators, Fan in Fan out, logic units, ADC's, TDC's, scalar and high voltage power supply unit. In the following chapters we shall be discussing all these modules with special attention to our application.

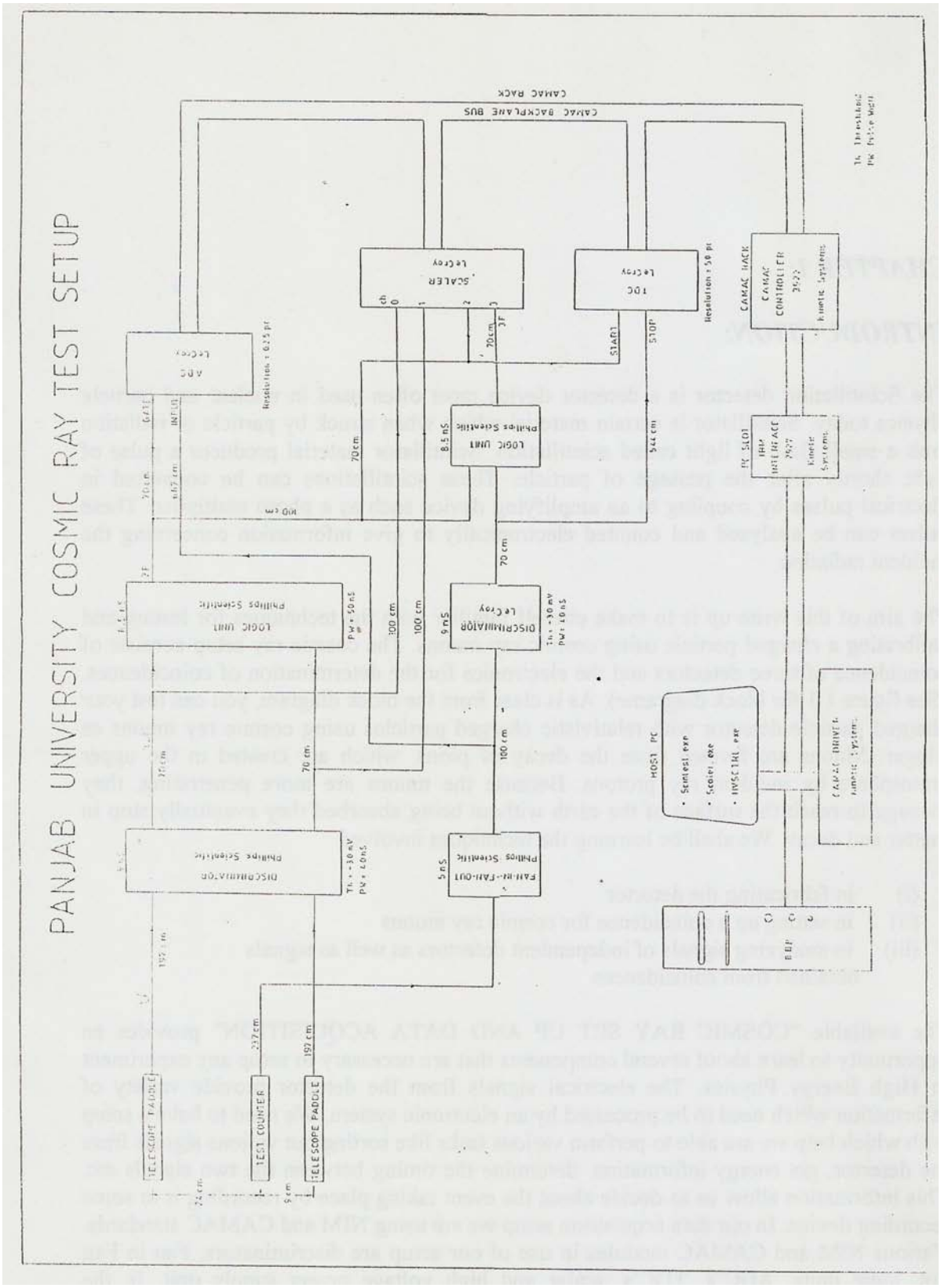



Figure 1.1: Block diagram of Cosmic Ray Set Up and Data Acquisition

## *CHAPTER 2:*

## *FABRICATION OF SCINTILATION COUNTER/DETECTOR TO BE USED AS PEDDLE:*

The scintillation detector is a special piece of plastic called a 'scintillator". When fast moving, charged particles, such as cosmic rays pass through the scintillator they excite the atoms in the plastic by giving them some energy. The excited atoms then lose this energy by emitting some photons of light. This light is detected by a sensitive piece of equipment called a "photomultiplier". [4]
The photomultiplier multiplies the small flashes of light into a large electrical signal that can be measured. From the size of the signal we can tell how many particles passed through the scintillator. The scintillator is coupled to the photomultiplier through light guide and is light tight packed so that only light detected is caused by the cosmic rays. [4]

## 2.1 SCINTILLATIOR MATERIAL:

A scintillator is material which "scintillates". It gives small flashes of light (photons) when a charged particle passes through it. There are lots of materials that act as scintillators. Types of scintillator material available are: Organic crystals, Organic Liquids, PLASTICS, Inorganic Crystals, and Gases & Glasses. In our case it is plastic scintillators (Organic) as shown in the figure 2.1. Some of the photons reflect off the highly polished surface, bouncing around the panel as shown. A fraction of the photons eventually emerge from the end of the panel and go into the light guide. Each passing muon creates about 20,000 photons in a 1 cm thick scintillator panel. [3]

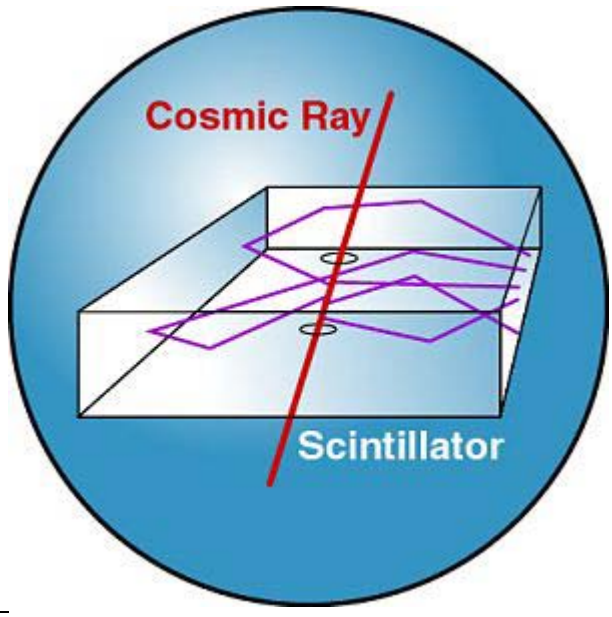



Figure 2.1: Passage of cosmic ray through the plastic scintillator

The property of scintillator material is called Luminescence which is of two types.

| | | |
|---|---|---|
| 1. | Flourescence: - | This is when emission occurs Immediately after the absorption. |
| 2. | Phosphorescence: - | This is if emission is delayed since Excited state is metastable |

## 2.2 PLASTIC SCINTILLATORS:

Plastic scintillators are most widely used in Nuclear and High Energy Physics (HEP). These are solutions of organic scintillators but in a solid plastic form. If an organic scintillator is dissolved in a solvent, which can then be subsequently polymerized, and an equivalent solid solution can be produced. Because of the ease with which they can be shaped and fabricated, plastics have become useful form of organic scintillator.

Most Common plastics are polyvinyl toluene, polystyrene and polyphenyl benzene. The primary solutes are p-teriphenyl and PBO. Secondary solute such as POPOP is added for wavelength shifting properties. Plastic Scintillator BICRON 404 is used in our High Energy Physics Laboratory. It is a general purpose Scintillator. The general characteristics of BICRON 404 Scintillator are given in the table. [5]

TECHNICAL DATA OF
GENERAL PURPOSE SCINTILLATOR: BICRON 404

| | |
|---|---|
| Base: | Ploy vinyltoluene |
| Density: | 1.032 |
| Refractive Index: | 1.58 |
| Coefficient of Linear Expansion: | $7.8X10^{-5}/^{0}C$ |
| Softening Point: | $70^{0}$ C |
| Specific Gravity: | 1.032 |
| Atomic Ratio: | ~1.1 |
| Wavelength of Max. Emission: | 408 nm |
| Light output: | 90% |
| Vapor Pressure: | May be used in vacuum |
| Solubility: | Soluble in aromatic solvents, chlorine, acetone etc Insoluble in water, dilute acids, lower alcohols etc |
| Rise time: | 0.7 ns |
| Decay Time: | 1.8 ns |
| Pulse FWHM: | 2.2 ns |

Plastic Scintillators have following properties:

- They offer an extremely fast signal with decay constant ( 2-3ns)
- They have high light out put.
- They are generally rugged, easily attacked by organic solvent such as acetone. When handling unprotected plastic, it is generally advisable to wear Cotton gloves as the body acid from one's hand can cause cracking of the plastic after a period of time.
- They are very flexible and easily machined by normal means

## 2.3 LIGHT GUIDE

For coupling of the scintillators to the Photomultiplier Tube (PMT) we need light guides as the same can not be coupled to the PMT directly because of the size of the scintillator. We use Perspex as light guide material which has the same refractive index as that of scintillators. The light guide is the shaped piece of plastic (Perspex) as shown in figure 2.2 below. It is designed in such a way that one end matches with the scintillator and the other end matches with the light sensitive area of the PMT. Photons entering the light guide from the scintillator will generally hit its surface at such an angle that they are internally reflected and are eventually directed into the photomultiplier tube.

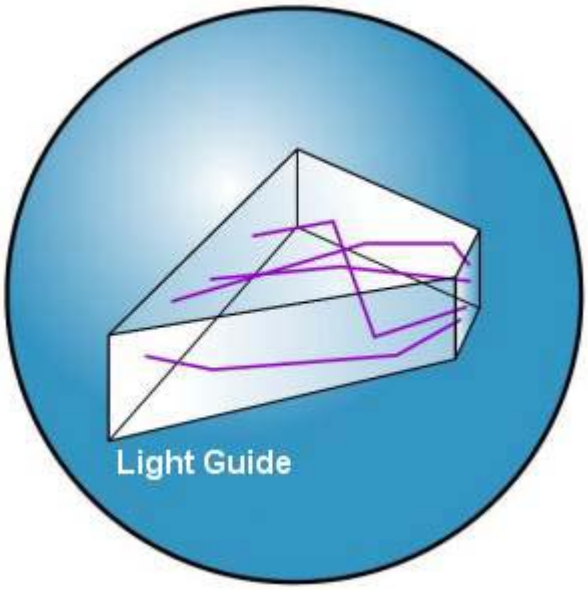



Figure 2.2: Light Guide

Light guides can be made in any shape, size and length as per the geometry required. For coupling the light guide to the circular face of the PMT we further couple the light guide to a circular disc made out of the same material as of light guide.

## 2.4 The Photomultiplier Tube [2]

The photomultiplier is extremely sensitive light detector providing a current output proportional to light intensity. Photomultipliers are used to measure any process which directly or indirectly emits light**.** Photomultipliers have distinct advantage over other light detectors because of large area light detection, high gain and ability to detect signals of single photons.

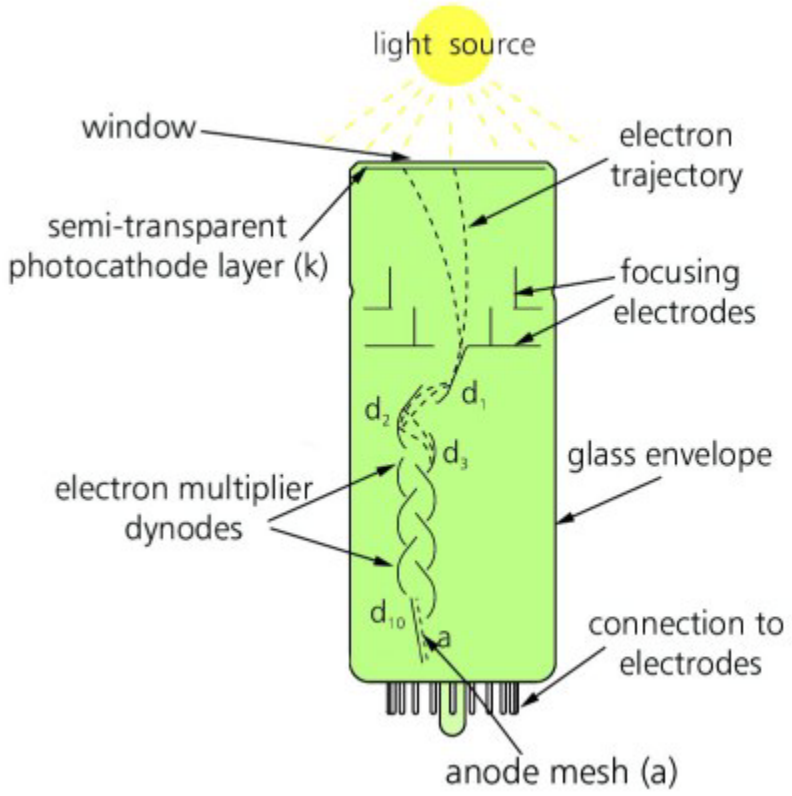



Figure 2.3: Operation of photomultiplier

The photomultiplier detects light at photocathode (k) which emits electrons by photoelectric effect. These photoelectrons are electrostatically accelerated and focused onto the first dynode (d1) of an electron multiplier. On impact each electron liberates a number of secondary electrons which are in turn, electro statically accelerated and focused onto the next dynode (d2). The process is repeated at each subsequent dynode and the secondary electrons from the last dynode are collected at the anode (a). The ratio of secondary to primary electrons emitted at each dynode depend upon the energy of the

Incident electrons and is controlled by the inter-electrode potentials. By using a variable high voltage supply and voltage network, to provide the inter-electrode voltage, the amplitude of the photomultiplier output can be varied over wide range.

Photomultipliers are available in range of geometry and size for the *active area of photocathode*. In the majority of types the active area has circular geometry. Some have reduced active area, achieved by electrostatic focusing, which can be an advantage in the detection of week light sources. In case of coupling the scintillator directly with PMT, a flat window is best. The photocathode is deposited as semitransparent layer on the inside of the window. There are several materials which are used for the photocathode. The choice of photocathode together with window type determines the wavelength detection range of the photomultiplier.

The part of photomultiplier which collects the photoelectrons is called electron multiplier. The electron multiplier is very low noise, high gain, wideband amplifier made up of wide range of four different structures. These are called *dynodes.* Depending upon the nature of application one has to make a choice between the two dynode surface materials i.e. oxidized beryllium copper (BeCu) and caesiated antimony (SbCs). The collected photoelectrons from the photocathode area are focused on to the active area of the first dynode. See figure 2.5.


Figure 2.4: The electron multiplier in a photomultiplier

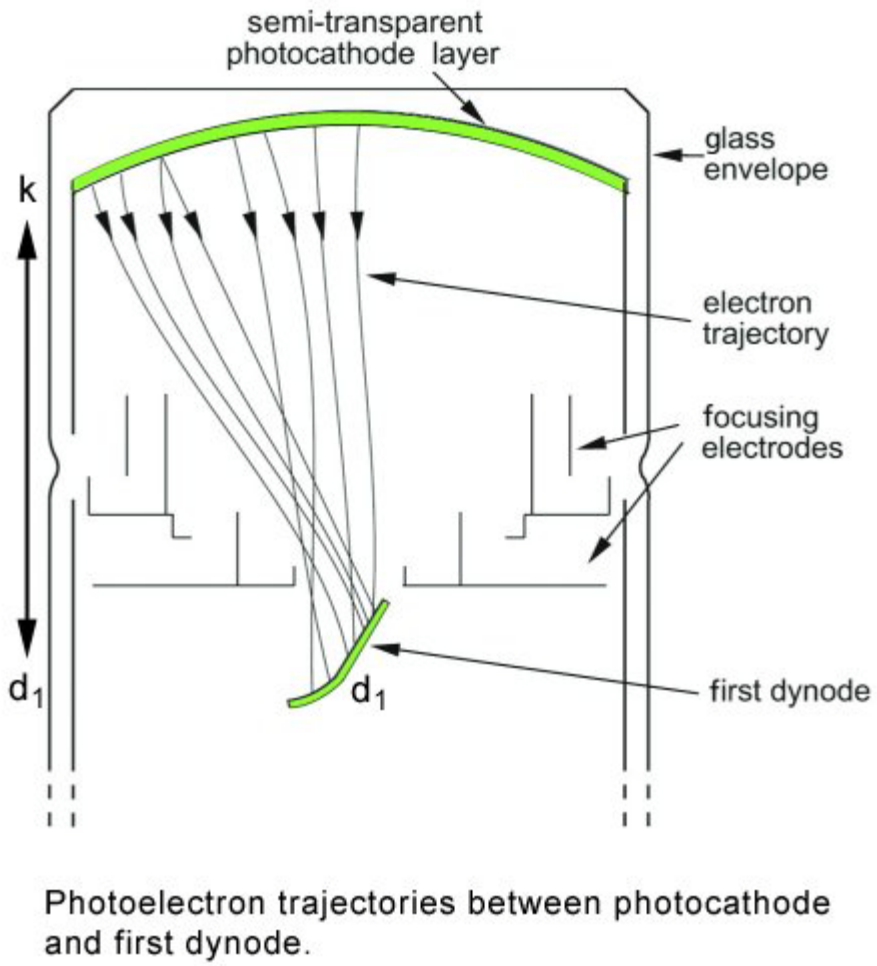



Figure 2.5: Focus of photoelectron onto the first dynode

The conversion efficiency for photons into photoelectrons depends upon the sensitivity of the photocathode. The relation between photocathode sensitivity and wavelength is called the *spectral response.* For the photocathode sensitivity we use terms such as quantum efficiency, radiant sensitivity and luminous sensitivity.

**Quantum efficiency** h (I) is the average percentage of incident photons that convert to photoelectrons.

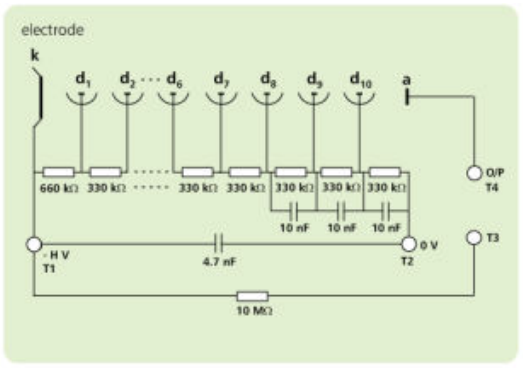
**Radiant sensitivity** (responsivity) E(I) is defined as the photocurrent emitted per watt of the incident radiation and is expressed in mA/W.

**Luminous Sensitivity (S)** It is a traditional unit for spectral response measured in units of mA/lumen. Value of S range from 20mA/lm to over 400mA/lm depending upon the type of photocathode.

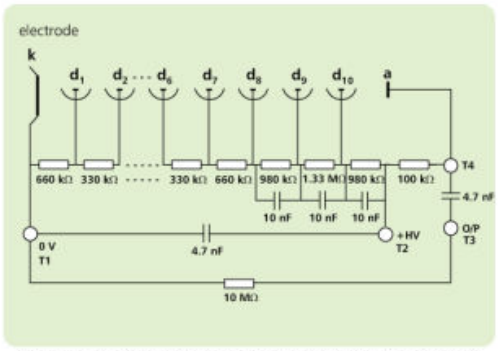
All photocathodes respond to white light for the value of S mentioned above. The manufacturer of photomultipliers however also gives parameters like Corning Blue (CB), Corning Red (CR) and Infra Red (IR) for the value of S.

*Gain* of photomultipliers is derived by the current amplification. Each dynode amplifies the incident electron current and overall gain is given by the product of the individual dynodes contribution. With many stages of gain, a small photoelectric signal is amplified to a measurable level. The gain of each dynode is related to the energy of the incident electron, and hence to the inter-dynode voltage.

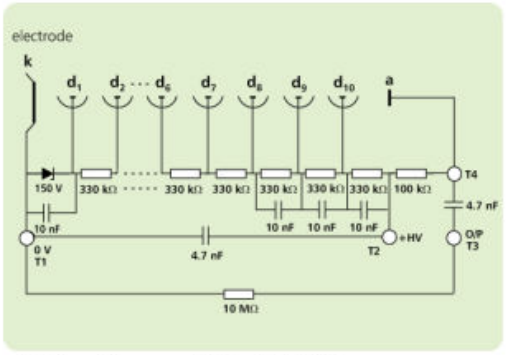
In general, a *single high voltage power supply* is employed, with a *resistive voltage divider network*, to provide suitable inter-electrode voltage. The more dynode stages in the photomultiplier, the higher is the gain at a specific overall applied voltage.



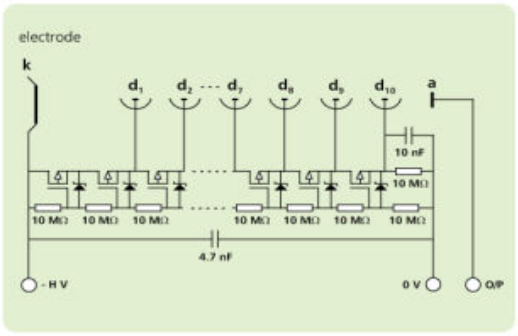

uniform resistive divider configured for -HV




tapered resistive divider configured tor +HV, showing decoupling capacitors for pulsed applications




divider with zener stabilised V(k-d1) configured for +HV




active uniform divider providing high performance and low power consumption over a wide dynamic range. Available only for -HV.

Figure 2.6: Different Voltage divider options for the photomultiplier

The first circuit in figure 2.6 above is known as uniform voltage divider, where inter dynode resistance is of the same value. In the second figure the resistance value increases towards anode. This is to overcome space charge which leads to non-linearity when dealing with high current pulses. For optimum performance V(k-$d_1$) is often higher than inter dynode voltage. In figure 3 a zener diode replaces the resister between k and $d_1$. This maintains V(k-$d_1$) constant regardless of the high voltage setting and ensures good collection and test response when photomultiplier is operated over a wide range of gain settings. A decoupling capacitor is to be connected across the three or four dynodes to provide transient signal charge. Figure four is an active voltage divider which ensures

constant gain up to a mean anode current of 100 $\mu$A, the maximum permitted in most of photomultipliers types.

The output from a photomultiplier is obtained even in absence of light input; this is referred to as dark current in dc application and dark count in pulsed application also referred to as background. The dark current varies considerably even, for photomultiplier of the same type.

- Dark current rate increases with photomultiplier diameter
- Dark current increases with temperature
- Dark current increases linearly with gain
- Dark count rate is independent of gain

## 2.4.1 THE EQUIVALENT CIRCUIT OF THE PHOTOMULTIPLIER AND THE OUTPUT SIGNAL [2]:

The appropriate equivalent circuit of a photomultiplier is an ideal current generator in parallel with output resistance $R_0$ and capacitance C0 (figure 2.7). Photomultiplier is a perhaps the device which conforms to the definition of an ideal source with $R_0$ in excess of $10^{12}$ Ω and $C_0$ in the range of 5-20 pF. The magnitude of $C_0$ depends on the type of tube used and circuit layout. The measured output depends upon the load resistance $R_L$ and capacitance $C_L$ in combination with $R_0$ and $C_0$.

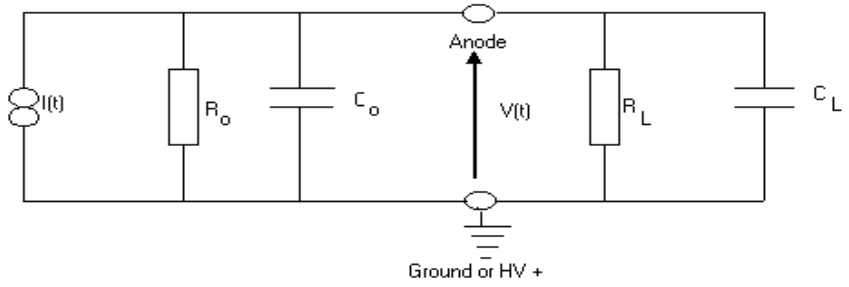



Figure 2.7: Equivalent circuit of photomultiplier

The following analysis shows how this capacitance together with the anode load resistance determines the nature of output signal.
The time constant of the circuit is: $\tau$ = RC where

$$R = \frac{R_0 R_L}{R_0 + R_L} \quad \text{and}$$

$$C = C_0 + C_L \quad \text{……..(1)}$$

Consider light output with an exponential decay in intensity, with single time constant, $\tau_S$ :

Photoelectron current is then given by:

$$I(t) = \frac{Ne}{\tau_S} \exp(-t/\tau_S) \qquad \ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Where N is the total number of photo electrons and the e = $1.6X10^{-19}$ C. For Ideal photomultiplier of gain G, the output I(t) is given by:

$$I(t) = Gi(t) \qquad \ldots\ldots\ldots\ldots\ldots\ldots(3)$$

Referring to figure 8, we have that the output voltage is

$$V(t) = \frac{NeGR}{\tau - \tau_S}[\text{expo}(-t/\tau_S) - \text{expo}(-t/\tau)] \quad \ldots\ldots.(4)$$

Where

N is the number of photoelectrons produced by light pulse,

E is the electronic charge

G is the photomultiplier gain

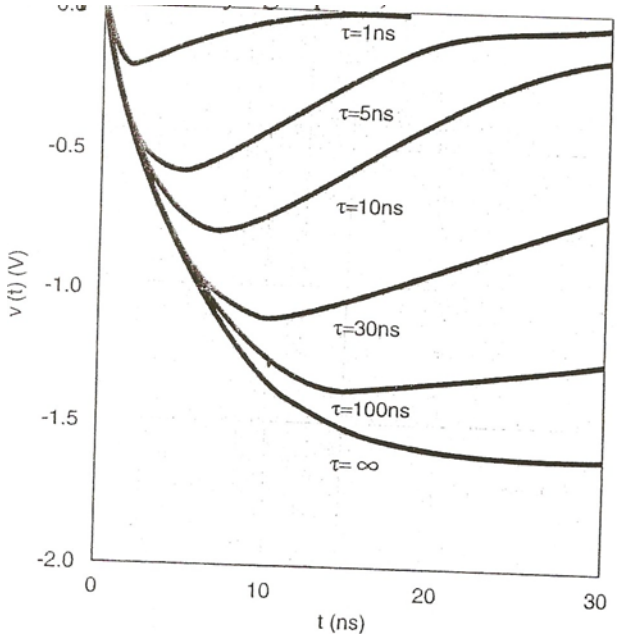



Figure 2.8: Output response curve for various time constants

Figure 2.8, shows the results of evaluating equation 3 for following parameters:

N = 100, G = $10^6$ , $\tau_S$ =5 ns, C = 10pF with resistance successively as 100, 500, 1K, 3K, 10K, and $\infty$ $\Omega$ (i.e. $\tau$ = 1ns, 5ns, 30ns, 100ns, and $\infty$ ns respectively). The maximum amplitude signal is obtained when R = $\infty\,\Omega$. In this case current is simply charging C and

$$V_0(t) = \frac{GNe}{C}[\text{expo}(-t/\tau) - 1]$$

Summarizing figure 2.8, we conclude as follow:

The output voltage is faithful reproduction of the input current I(t) when $\tau << \tau_S$.

In case of $\tau = \tau_S = 5$ ns, I(t) has decayed to 1% of the initial value, $V_0(t)$is still ~ 10% of $V_{max.}$ In other words the output pulse has a long tail, which increases with $\tau$.
When $R \leq 100\ \Omega$, implying $\tau << \tau_S$, the pulse is not integrated. This is "current mode operation".
When $R \leq 100\ \Omega$, implying $\tau << \tau_S$, the pulse is integrated. This is termed "voltage mode". Rise time increases as "voltage mode" reaches and in extreme case with $\tau$ - $\infty$, the voltage rise time is equal to the input decay time.
A long time constant $\tau$ is suitable for low event rates; if the rate ~ 1/ $\tau$ "pulse pileup" occurs.
When the photomultiplier is connected by matched coaxial cable of $50\,\Omega$ impedance to an external circuit, the peak value is ~100 mV, for parameters previously assumed.

## 2.5 SCINTILLATION DETECTOR MOUNTING & OPERATION [1]

We shall be fabricating the scintillation detector by coupling the two main components i.e. Scintillator and the PMT using light guides in between. The detector is then to be checked for its efficiency and put to operation. We will call this detector a paddle. Paddle consists of a rectangular shaped plastic scintillation detector, a fish-shaped light guide and 2 inch diameter and photo Multiplier Tube (EMI 9807B). For optical contact, optical glue ( Bicron 600 ) is to be used. For efficient collection of emitted photons and transporting them to the PMT, the Scintillator is to be wrapped with provided Tyvek paper and the entire paddle is to be wrapped with layers of black paper (Tedler) and black tape. Figure 2.9 shows various components we have used for making of such detector to be used as paddle.

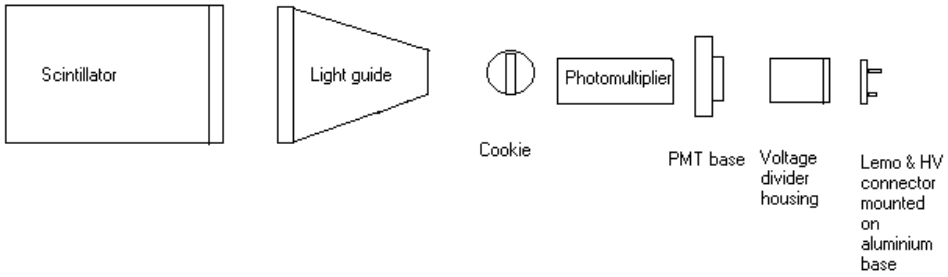



Figure 2.9: Components of Scintillator detector

Individual components of the detector i.e. the photomultiplier, plastic scintillator and the light guide are discussed in details in previous sub chapters 2.2, 2.3, and 2,4 respectively. 10 mm thick scintillator component is cut into 250X150 mm size and all the side are

polished. Similarly the fish tail is made of Perspex sheet of size 150X150 mm and of 10 mm thickness. For coupling Scintillator and the light guide, the joining edge of both the components are given L shape cut and held together with the help of optical glue as shown below in the figure 10. Figure also explains the attachment of the cookie with the other end of the light guide, which is of the size equal to the photomultiplier. We assemble the photomultiplier with voltage divider separately by using a aluminium housing for divider network and Perspex coupling for mounting the photomultiplier base as shown in the figure 2.10 above. HV and Lemo connector is mounted on a separate aluminium coupling. We shall be describing step by step mounting of the whole detector separately.

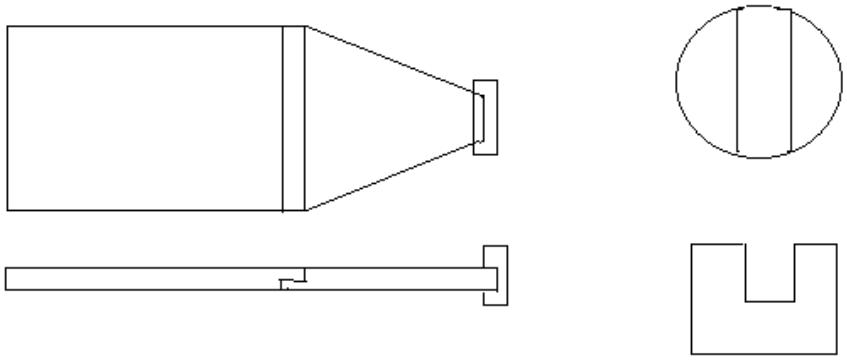


Figure 2.10: Coupling of Light Guide to the Scintillator

While mounting the detector, two most crucial points are to be considered:

- Light Collection
- Light Transport to Photomultiplier

The mounted detector is of no use if the scintillation photons emitted are not transferred or fraction is transferred to the photomultiplier. It is therefore important to collect maximum number of scintillation photons and transport to the photomultiplier photocathode.

Light in the scintillator can escape through the boundaries or can be absorbed by the scintillator itself due to attenuation length of the scintillator. The light absorption may be negligible in case of small detectors. However if the detector is big so that dimensions are comparable to the attenuation length, the absorption plays a big role. The typical attenuation length is of the order = 1m or more. [1] Since we are mounting a very small detector, there is no loss of light. However the loss of light does occur by transmission through the scintillator boundaries as illustrated below in the figure 2.11.

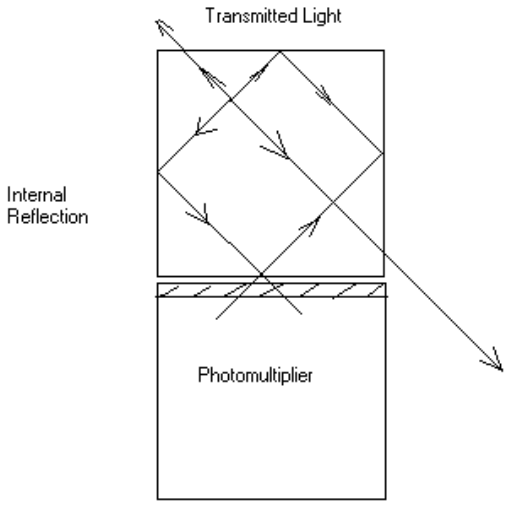



Figure 2.11: Light Collection in Plastic Scintillator

The light emitted at a given point in the scintillator, travels in all directions so that only a fraction of it is directly reaching the photomultiplier. Depending upon the angel of incidence light traveling to boundaries is either turned back to the scintillator due to the internal reflections or transmitted out.

The losses described above reduce the efficiency of the detector. We have to therefore find out some way of increasing the efficiency of light collection. The simplest way is to redirect escaping light by external and /or internal reflection.

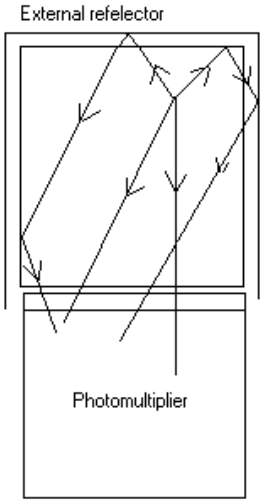



Figure 2.12: Scintillator with an external reflector for improvement of light collection

As is clear from the figure 2.12 the light which was previously transmitted out is now directed back to the scintillator and then to the photomultiplier by making one or more reflections with the help of external reflector. We use either alluminium foil or MgO, $TiO_2$ alluminium oxide in form of powder or paint. We also polish the surface of the scintillator to have internal reflections at the same time. We therefore use the polished scintillator and wrap it with alluminium foil followed by light tight layers of black paper. White tyvec reflecting paper has been found to be a replacement to the aluminium foil.

Coupling between the photomultiplier and scintillator is done using light guide in between, described earlier. While mounting the detector, we have to first couple scinitillator to the light guide and then the light guide to the photomultiplier. For making the optical contact between the two media i.e. photomultiplier and the Perspex we use silicon grease or oil because the refractive index is very close to that of scintillator. Optical glue 600 from Bicron is used to join the scintillator with light guide, refractive index of which is also close to the refractive index of scintillator and of the Perspex.

## 2.6 LIST OF COMPONENTS/MATERIAL RQUIRED FOR MOUNTING THE SCINTILLAOR DETECOR:

1. Scintillator, cut into rectangular shape (size 250x150mm)
2. Light guide, (Perspex) cut into fish tail shape (size 150X150mm).
3. Cookie (round) cut into the size of photomultiplier ( 2”dia ).
4. Two Aluminum strips for fixing the scintillator with light guide.
5. Optical Glue Bicorn 600.
6. White reflecting paper (Tyvek) for wrapping
7. Black paper (tedler) for 2$^{nd}$ wrapping of whole peddle.
8. Photomultiplier Tube (PMT) 9807B.
9. Voltage divider for PMT EMI 9807B.
10. Aluminum Housing for PMT 9807B.
11. Aluminum Housing for voltage divider of PMT.
12. Fixed Lemo socket ERA.00.250 CTL.
13. HV Connector/ socket (MHV Type).
14. Co-axial cable CCE.99.281.505 (LEMO).
15. Silicon grease
16. Aluminum foil tape.

## 2.7 MOUNTING/FABRICATING THE DETECTOR TO BE USED AS PEDDLE

Following steps illustrate the practical example of how to mount a simple plastics scintillation counter to be used in Laboratory:-

Step 1

Keep the material ready: Scintillator, PMT, PMT Base, alluminium housing for both PMT & Base, light guides, cookie, black taps, black paper, reflecting paper like Tyvek, optical glue etc

Figure 2.13: Materials for detector assembly

Step 2

Attach the scintillator with light guide with the help of optical glue Also attach the cookie with the help of same optical glue with light guide. Give some time for the optical glue to solidify and let the three parts join/couple properly.

Step 3

Apply the aluminium foil tape to all the sides of the scintillator as well as light guide. This aluminum tape shall work as reflector and help in reflecting back the light into the scintillator and further to PMT through the light guide.

Step 4

Now wrap the whole detector neatly in Tyvek (reflecting paper). Special care is to be taken that the detector is covered properly as the corners and sharp bends where light leaks will most likely occur .

Step 5

Another wrapping of the whole detector is to be done by using black tedler paper and black tape in the same fashion as described in step 4.The detector is now ready to be tested.

Figure 2.14: Wrapped in tyvec & tedler

Step 6

Assemble the voltage divider using Lemo socket and HV socket with help of the aluminium housing provided for it. Solder the HV wire and signal wire with the respective sockets.

Figure 2.15: Assembling the HV divider

Step 7:

Plug in the EMI Tube to voltage divider socket. Clean the whole assemble including the face of PMT of any old grease or dirt.

Figure 2.16: Assembled PMT with divider

Step 8:

Apply some optical grease to the face of PMT and attach it with cookie of the wrapped scintillator in step 5 with the help of aluminum coupling provided for the purpose. Use black tape to fix cookie and PMT with coupling. The detector is now ready to be put to operation.

Figure 2.17: Assembled detector as peddle

## 2.8 TESTING OF PEDDLE:

The mounted Peddle need to be tested to ensure for its proper working. The best way is to test the same by placing a suitable source upon the peddle and viewing the signal directly on O'Scope.

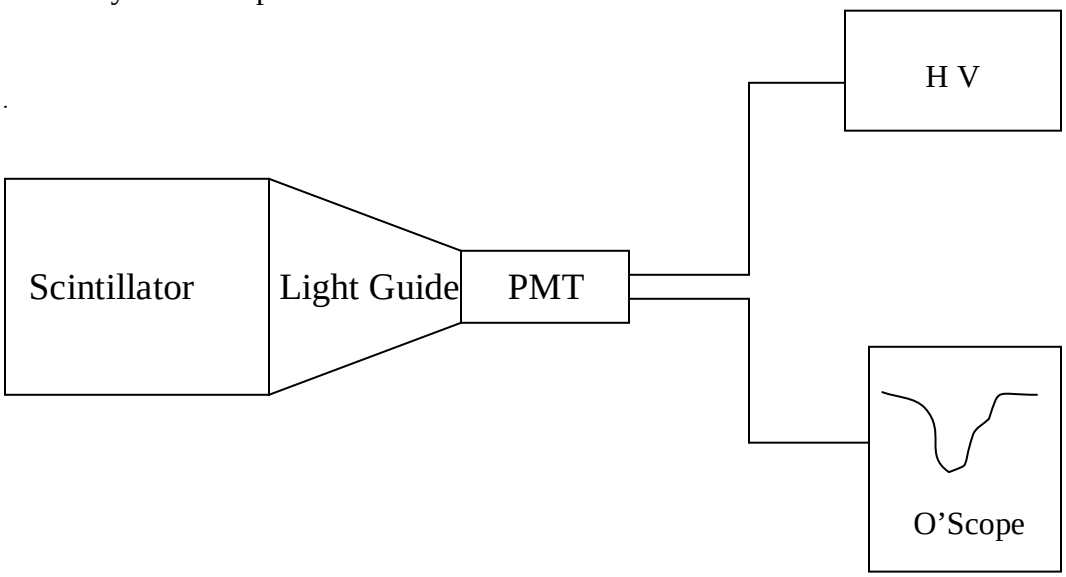



Figure 2.18: The set-up for testing of the assembled detector

However if the radio active source is not available during the experiment, we shall be testing the mounted peddle with the help of Cosmic Ray. By applying the recommended optimum voltage (=1650V) to the PMT, we shall be able to observe a well formed signal on O'Scope.

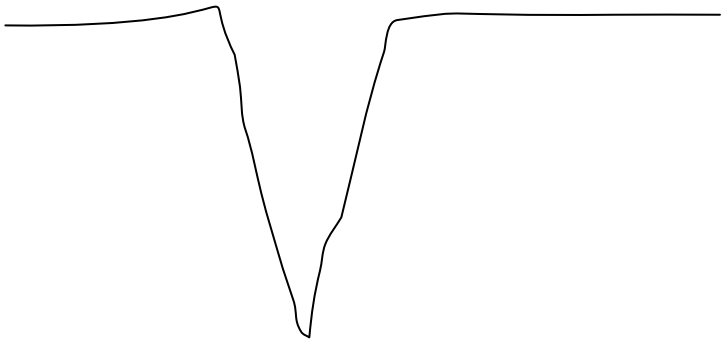


Figure 2.19: Signal from the Plastic Scintillator

The signal on O'Scope should have maximum height and low noise. Recommended noise should not be more than 40mv in the optimum voltage of the PMT. If there is no signal or week signal or distorted signal obtained on O'Scope, this should be due to many factors while assembling the peddle i.e.

-Bad optical coupling to the Scintillator
-Bad coupling of PMT to the Cookie
-Bad wrapping of the detector
-Bad PMT base or voltage divider
-Bad cable connection

We shall be checking the detector for light tightness by first observing the signal in open and then after covering it with black cloth. Comparing the two signals, we shall be able to decide how good the peddle is being fabricated. Steps are to taken to modify or correct the packing part of the whole peddle for better results. Testing the peddle for efficiency is described in the following chapter.

## 2.7 FINDING OUT THE OPTIMUM WORKIG VOLTAGE OF THE PHOTOMULTIPLIER:

The pulse height of the counter detector depends upon the applied voltage to the photomultiplier. It is recommended to stay within the range (upper and lower) given by the manufacturer. During the testing of the mounted detector, we had been able to observe a well formed signal by applying the upper and the lower limits of the voltages given by the manufacturer. For finding the optimum voltage of the photomultiplier, however we shall be using the counting technique. Photomultiplier signal is analyzed by a discriminator to find out the optimum voltage. We shall be using a setup shown in diagramed figure2.20 for this purpose.

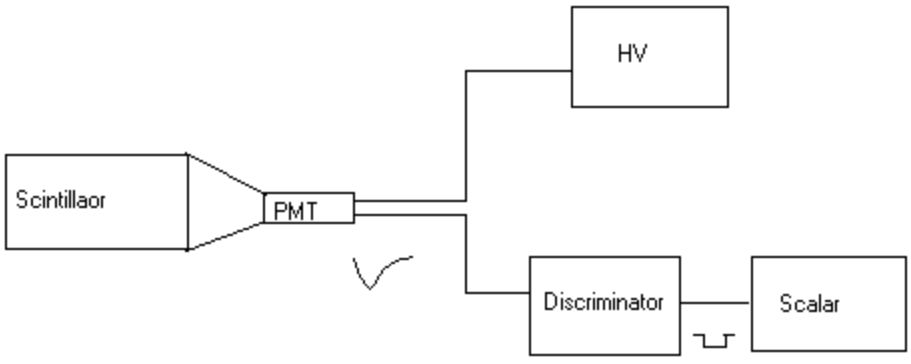



Figure 2.20: Set-up for optimizing the high voltage for the photomultiplier

We shall start with the lower voltage end and register the counts for minimum 5 minutes. Very few counts shall be registered as the pulse heights are too small to pass through the discriminator. The counts start rising sharply as we increase the voltage. At certain stage, these counts shall be same for a particular range of voltage. After this range, however the counts rise sharply once again. If we draw a plot between various counter reading corresponding to voltages, we find that plateau rises sharply up to a certain voltage range and becomes flat over a certain region in the middle. By fixing the voltage in the middle of the flat plateau we get the actual working voltage of the photomultiplier. At this stage there is a minimum variations due to drift in photomultiplier gain or voltage supply

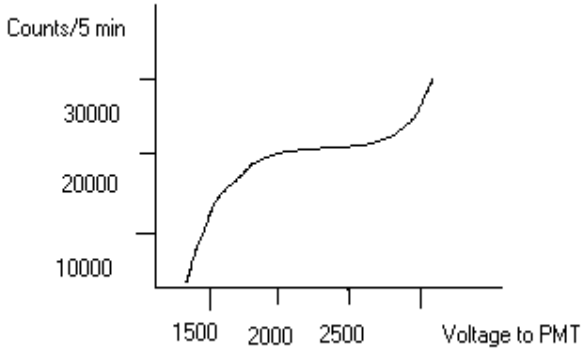



Figure 2.21: Counts verses voltage plateau

## *CHAPTER 3:*

## *THE SETUP FOR SIGNAL FORMATION IN SCINTILLATION COUNTERS, SIGNAL PROCESSING & DATA ACQUISITION:*

The development of detector system is an interdisciplinary mix of physics and electronics. For understanding the scintillation detectors in high energy physics, we requires knowledge of the low noise electronics techniques, analog and digital electronics, high speed data transmission and computer based data acquisition system. The radiations in a detector provide variety of information in the form of electrical signals. These information need to be processed by an electronic system. We therefore need to have an electronic system with which help we are able to perform various talks like sorting out various signals from the detector get energy information, determine the timing between the two signals etc. This information allows us to decide about the event taking place by recording it to a recording device. We have to understand some techniques to setup an electronics system for performing various experiments in high energy particle physics. For performing basic processing functions e.g. amplification, discrimination etc., nuclear electronics has been standardized into modular form. Each module is made up of standard electrical and mechanical specifications. These modules can be interconnected with each other as per requirement. NIM and CAMAC are two standards accepted throughout the world so that modules from different laboratories can be freely exchanged without any problem in compatibility. We shall learn and discuss basics of various standard modules in this chapter and the technique involved in using them.

The setup is divided into four main parts:

1. The Scintillation-Counter-Setup for Signal formation and detection of particle using cosmic muon as trigger.
2. High Voltage Supply Setup for various Photomultipliers coupled to each detector.
3. Electronics Setup for pulse signal processing
4. The Data Acquisition Setup for recording events and processing signals

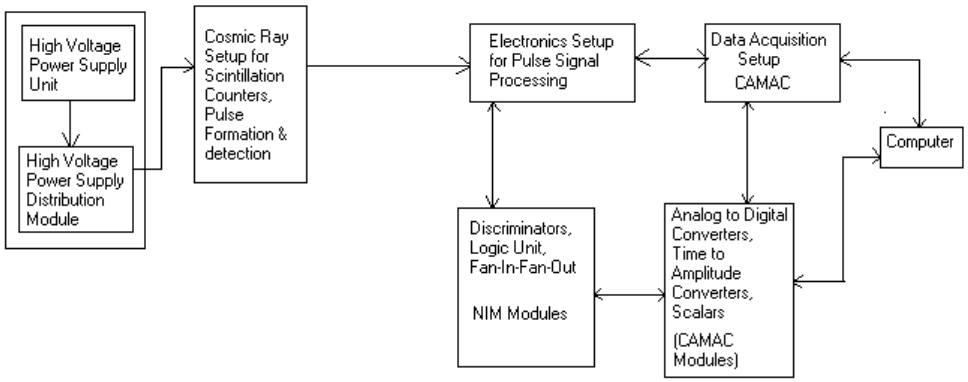



Figure 3.1: Setup Schematic

## 3.1 COPONENTS USED IN THE SETUP:

1. Scintillation Peddles
   (Bicron Scintillator optically coupled to Photo Multiplier Tube from EMI)
2. High Voltage (HV) DC Power Supply (Model 2415 from LeCroy & Model N 126 from C.A.E.N)
3. NIM Power Bins ( Model TB 3 B Oxford)
4. NIM Power Supply (Model TC 911-6 Oxford)
5. Camac Crate (Model 1502 from Kinetics)
6. Camac Crate Controller (Model 3922-ZIB from Kinetics)
7. Discriminators (Model 705 & 706 from Phillips and Model 623B from LeCroy)
8. Linear Fan-In-Fan-Out (Model 428 from LeCroy)
9. Logic Unit (Model 365 AL from LeCroy)
10. Scalar (Model 2251 from LeCroy)
11. ADC ( Model 2249A from LeCroy )
12. TDC ( Model 2228 A from LeCroy)
13. Co-axial Cables
14. O'Scope
15. IBM PC

## 3.2 THE SETUP FOR SIGNAL FORMATION AND DETECTION OF PARTICLES USING COSMIC MUONS AS TRIGGER

## SCINTILLATION DETECTORS:

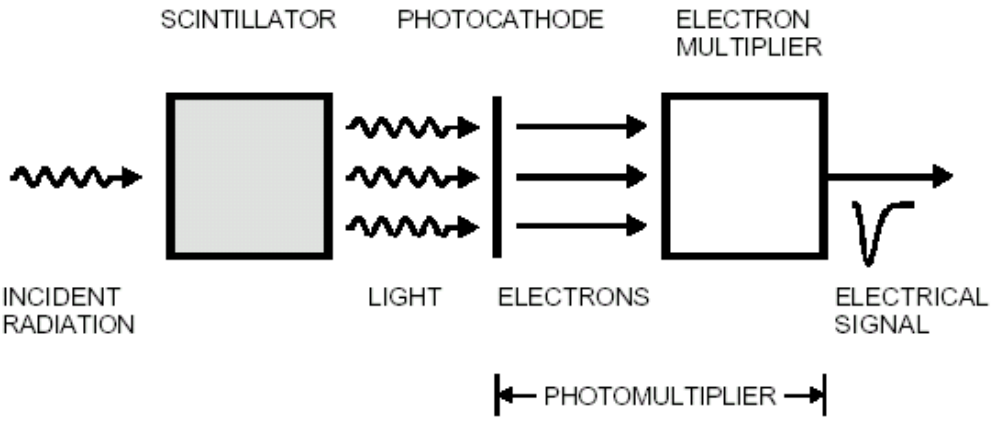



Figure 3.2: Schematic of Scintillation Detector

Plastic Scintillator Detectors provide electrical signal output as shown above. The principal functions of the detector are explained above in the schematic diagram figure 3.2. We have already learnt how to assemble such detector. (Refer to Chapter 2 "Assembly of Scintillation Counter Detectors to be used as Peddles")

Figure 3.3 : Scintillation Detector as a Standard Peddle

Figure 3.3 Shows the Assembled Scintillation Detector as Standard Peddle which is made up of plastic scintillation material cut into rectangular size, a fish shaped light guide and a 2" diameter PMT (EMI). For coupling the light guide to the Photomultiplier, a cookie of 2" diameter is attached to the light guide on one side with the help of optical glue. The other side is coupled with the Scintillator with the help of the same glue. Optical Grease is used for making optical contact between PMT and the cookie. The whole assembly is wrapped with the tyvec and teddler paper for efficient collection of emitted photons and transporting them to Photomultiplier.

## THE COSMIC RAY SETUP:

Since we need to detect particles from the cosmic rays, a setup is to be established for the Scintillator Counters. This part of the setup is nothing but a geometrical arrangement of one, two or more detectors in a light tight rack (Counter Rack) as shown in figure 3.4, for detections and formation of the signal of independent detectors as well as the formation of signals 2 fold, 3 fold or more fold coincidences. High Voltage Cabling is done for each photomultiplier through the distribution box (Refer to 3.3) inside the Counter Rack. The signal cables are taken out of the rack and are wired to the electronics for further processing. Two standard peddles are placed on two separate compartments of the rack in such a way that their area of cross section match with each other. The counter under test is placed in between the two peddles and cosmic mouns are allowed to pass through all.

Figure 3.4 : The Adjustable Scintillation Counter Rack in CMS/D-Zero Lab for Cosmic Ray Setup at
Panjab University

## 3.3 HIGH VOLTAGE (HV) DC POWER SUPPLY:

Each Photomultiplier attached to scintillation peddle need a well regulated High Voltage Power Supply for its operation. While selecting High Voltage Power Supply following few points are to be considered:

- Photomultiplier operate over a range of positive or negative high voltage-spanning 300 to 3000 V, depending upon the Tube type and application
- Photomultiplier gain varies rapidly with applied voltage requiring a high degree of sensitivity control and long term stability DC Supply should operate with low ripples
- Photomultiplier we have used for our peddles need to be operated on +ve High Voltage. A well regulated DC Power Supply Model H3K05P from Aplab is in use for the described setup.

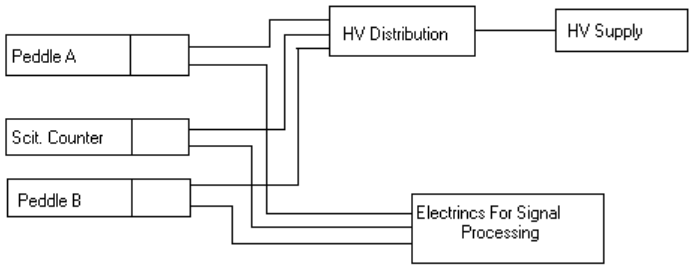



Figure 3.5 High Voltage Connections through distribution module using Single Supply

HV need to be applied to three or more Photomultiplier at a time in our setup. So a distribution box is being developed and made to feed the required HV for operating each Photomultiplier. The interconnections of more than one detector via this HV distribution box is explained in figure 3.5. Ten number of Zenor Diodes of the type $V_z$ =30V, 1W are used. EHT connectors are connected to these Zenor Diodes through resisters of value 10K, 0.5W, 1%.The EHT connectors are mounted on the aluminium sheet as shown. As per the wiring shown, at each EHT connector, distributed voltages are available. Voltage drop on each connector with the arrangement is mentioned on each connector. So for a given input HV supply to the distribution box, the voltage mentioned on each connector is to be subtracted before connecting to each PMT. This way we are able to apply the required HV to each PMT. The electrical and mechanical details of the EHT module are given in the attached diagram figure 3.6.

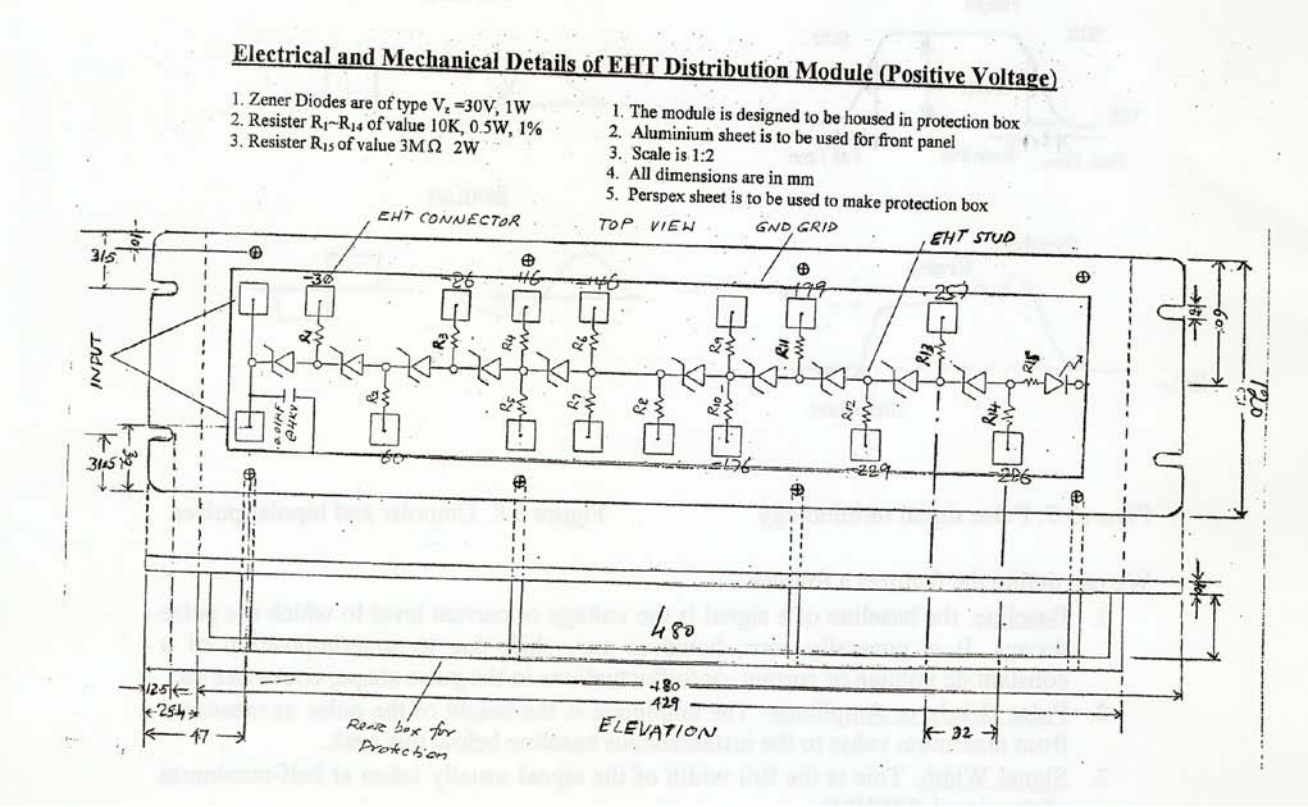



Figure 3.6: Electrical and Mechanical details of EHT distribution Module

## 3.4 PULSE SIGNALS IN NUCLEAR ELECTRONICS:

Nuclear Electronics deals with electronic techniques which are closely associated with radiation measurement. The detectors supply directly electronic signals (electric charge) when they detect nuclear radiation. The purpose of the Nuclear electronics is processing of detector signals in order to supply quantitative information about the different characteristics of radiation.

The coding of information in nuclear electronics is in the form of pulse signals. These are surges of current or voltage in which information is contained in one or more of its characteristics, for example its polarity, amplitude, shape its occurrence in time related to another pulse, or simply its mere presence. Particle detectors are pulse devices. Figure 3.7 shows an ideal rectangular pulse, either in voltage or current, as a function of time.

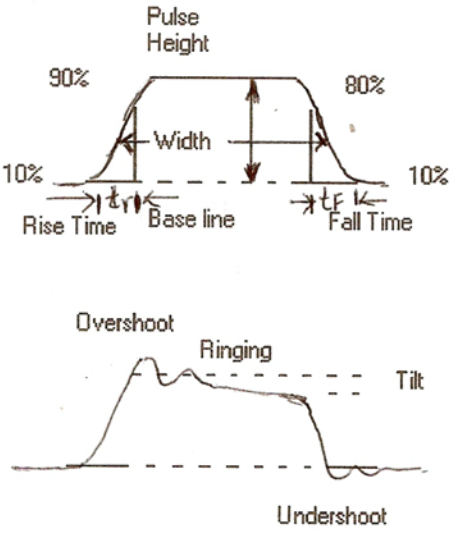



Figure3.7: Pulse signal terminology

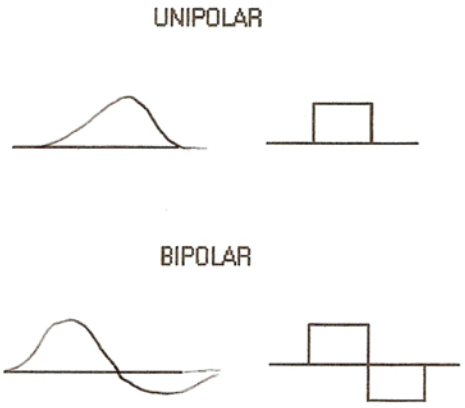



Figure 3.8: Unipolar and bipolar pulses

We can define the features a follows:

1. Baseline: the baseline of a signal is the voltage or current level to which the pulse decays. It is generally zero, however may shift due to superimposition of a constant dc voltage or current, or to fluctuations in the pulse shape, count rate etc.
2. Pulse Height or Amplitude: The amplitude is the height of the pulse as measured from maximum value to the instantaneous baseline below this peak.
3. Signal Width: This is the full width of the signal usually taken at half-maximum of the signal (FWHM).
4. Leading Edge: The leading edge is that flank of the signal which comes first in time.
5. Falling Edge: The falling edge or tail is that flank which is last in time.
6. Rise Time: This is the time which determines the rapidity of the signal and is important for timing application.

7. Fall Time: Fall time is the time taken for the signal to fall from 90 to 10% of its full amplitude.
8. Unipolar and Bipolar: Signal pulses are both unipolar and bipolar. Unipolar pulse is the one which has one major lobe on one side of the base line. Bipolar pulse cross the base line and form a second major lobe of opposite polarity. Figure3.8 illustrates these two types of pulses.

Practically it is found that pulses are often distorted because of various factors in the circuit. Figure also illustrates such deviated pulse.

## 3.4.1 ANALOG AND DIGITAL SIGNALS:

Signals carry information in two forms: analog or digital.

Signals which continuously vary with time are analog signals. Analog signals carry continuous valued information by varying one or more of its characteristics e.g. amplitude or shape. A scintillation detector as we know generates pulses whose amplitudes are in proportion to the energy deposited in detector. If a beam of particles with a continuous spectrum of energy is allowed to strike a detector, then a continuous analog signal spectrum of pulse heights will result. If we consider each possible amplitude or shape of a pulse as a state, then the analog signals can be said to have an infinite, non-countable number of states.

Digital signals have only two possible levels of states: present or not present. The information contained in a digital signal is quantized in nature. For example signal from a scintillation counter has essentially two states signal present or not present. Corresponding information is then simply: yes, radiation was detected, or no, radiation was not detected. No finer distinction is possible. All logic signals are limited to two states only.

Though, a logic signal carries less information than analog signals, it is more reliable since exact amplitude or form of the signal need not to be perfectly preserved. The distortion or noise which is always present in any circuit will alter the information in an analog signal but would have very less effect in the logic signal. As the logic signals carry limited information, equivalent analog information can be obtained by using several logic signals. Each logic signal would represent a digital number whose value corresponds to the analog information. Since there are two states the number must be binary system. The logic pulse present would represent binary 1, while the pulse absent would represent 0. An entire binary number would then consist of a string of logic signals, which would be transmitted serially, i.e. one after the other or simultaneously along an equal number of parallel-lines.

In Nuclear Electronics, the two electrical states of logic are standardized to NIM convention. One logic state is 0 when no pulse and the other is a fixed voltage level. As it is difficult to generate a pulse with exact right voltage level, a band of voltages into which signal must fall is defined instead. So, analog signals from detector are changed into logic signals at sometimes or another in nuclear electronics. Discriminators as discussed earlier are used to detect signals from detectors which radiate signals with variable amplitude. However, where, the signal need to be digitized, for exact amplitude, analog to digital converters are used (ADC's). Similarly digital signals are converted into analog signals with the help of digital to analog converters.

### 3.4.2 FAST AND SLOW SIGNALS:

Fast signals generally refer to pulses with rise time of few nanoseconds or less while slow signals have rise time on the order of hundreds of nanoseconds or greater. This is true for both linear logic signals. For timing applications and high count rates the fast pulses are important. It is important to preserve their rise time throughout the electronics system. Slow pulses, are generally less acceptable to noise and offer better pulse height information for spectroscopic work. Fast signals are to be treated differently than slow signals. It is because of their great susceptibility to distortions from small, stray capacitances, inductances and resistances in circuit and interconnections. These circuits can combine to form parasitic circuits; for example RC or RL circuits which have fast transient response due to small values of R, C and L. Compared to slow signals, these transients are negligibly short. Compared to fast signals, these transients are of the same order of magnitude and duration. A fast signal passing through one of these circuits can thus be quickly deformed.
Another problem is the distortion from reflections in the interconnecting cables. This arises because of the short duration of fast pulses relative to their time of transit in the interconnecting cables. Special attention is therefore to be taken not only in circuit design but also in the interconnecting cables.

### 3.4.3 THE FREQUENCY DOMAIN, BANWIDTH:

Frequency component in pulses is another point to be taken care of while describing a pulse. From Fourier analysis we know that pulse can be decomposed into superposition of many pure sinusoidal frequencies. If we have a pulse whose shape in time is represented by function f(t),where t is time, then

$$f(t) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} g(\omega) \exp(i\omega t) d\omega \qquad \text{.....(3.1)}$$

where $g(\omega)$ is the Fourier transform or frequency spectrum of the pulse. Inverting the equation 3.1 we have,

$$g(\omega) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} f(t) \exp(-i\,\omega t) dt \qquad \text{.....(3.2)}$$

Let us now consider a an ideal rectangular pulse of width T shown if figure 3.9. The pulse is centered at t = 0, Thus,

$$f(t) = \begin{cases} A & |t| < T/2 \\ 0 & |t| > T/2 \end{cases} \qquad \text{.....(3.3)}$$

By Fourier analyzing this function we find spectrum

$$g(\omega) = \frac{1}{\sqrt{2\pi}} \int A \exp(-t\omega t) dt = \frac{AT}{\sqrt{2\pi}} \frac{\sin(\omega T/2)}{(\omega T/2)} \qquad \text{.....(3.4)}$$

Spectrum is plotted in figure 3.9 as a function of frequency f = $\omega/2\pi$. We observe that f(t) is a continuous spectrum of frequency component from 0 to $\infty$. Energy or power contained in each frequency component is the square of g($\omega$):

$$E(\omega) = |g(\omega)|^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(3.5)$$

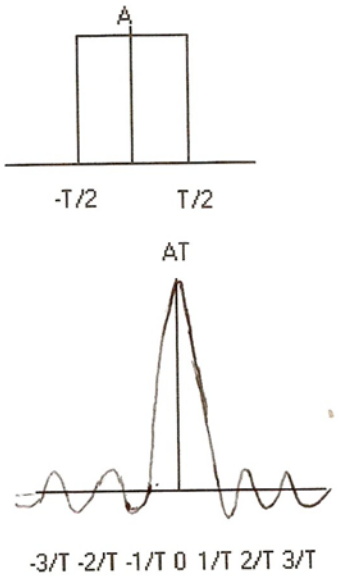



Figure 3.9: Fourier spectrum of a rectangular pulse

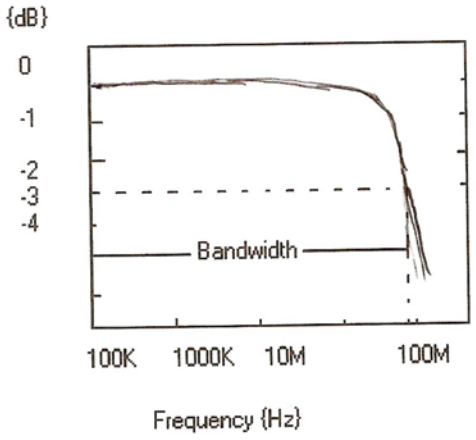



Figure 3.10: Frequency response curve and bandwidth

All frequencies play a roll in shaping of the function f(t). Therefore the electronic device must be capable of responding uniformly to all finite frequencies.

In real circuits, however, there exists a resistive and reactive component, which will filter out some frequencies so that response will always be limited to finite range in frequencies. This limited range is called Bandwidth. Figure 3.10 shows a typical response curve. The frequencies outside this bandwidth range are attenuated or cutoff.

Figure 3.11 shows the resulting pulse shapes obtained by integrating 3.4 from f = 0 to various cutoff frequencies.

A minimum bandwidth of $\Delta f \geq 1/T$, is necessary to give reasonable approximation of the pulse.. Comparing various figures it can be seen that the high frequency component allows the signal to rise sharply, while the lower frequency account for the flat parts. For typical fast pulse of say 5 ns width this would mean $\Delta f \geq 200$ MHz. For slow pulses this limit is lower. Fast nuclear electronics therefore should be able to accept frequencies up to = 500 MHz. For nanosecond pulses, it can be shown that frequencies up to = 100 kHz can be removed with no harm. In nuclear electronics, only frequencies between = 100 kHz and = several hundred MHz to 1 GHz are important.

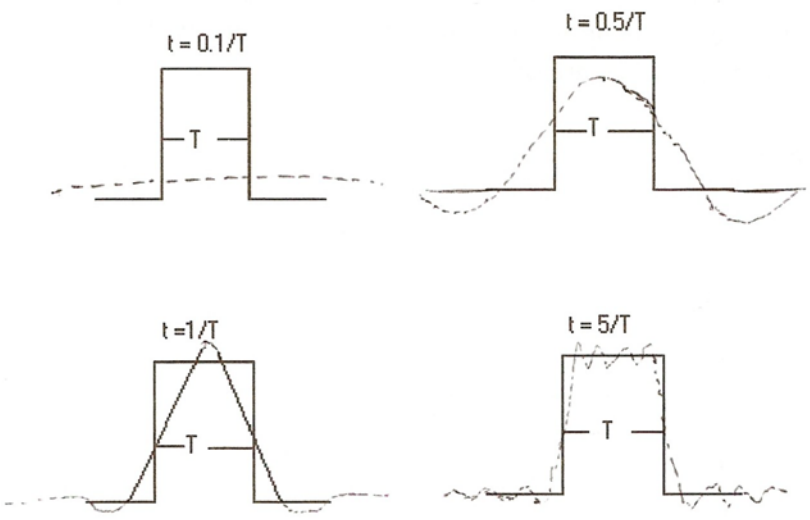



Figure 3.11 Effect of limited bandwidth on a rectangular pulse

## 3.5 NIM POWER BIN AND NIM STANDARD:

NIM means Nuclear Instrument Module. It is a standard established for the nuclear and High Energy Physics. NIM Standard is used for fast trigger and Logic operations as well as signal conditioning. The bin provides mounting space and power source for up to 12 NIM Modules. Bin is designed and constructed with connectors for each module position providing standard NIM power supply voltage of +6V, -6V, +12V, -!2V, +24V, -24V dc. Input supply to the bin is 220V ac. The control panel includes an ON/OFF switch, a power monitor lamp, voltage test point and a temperature warming lamp which indicate that the temperature of the power supply is approaching the design limit.

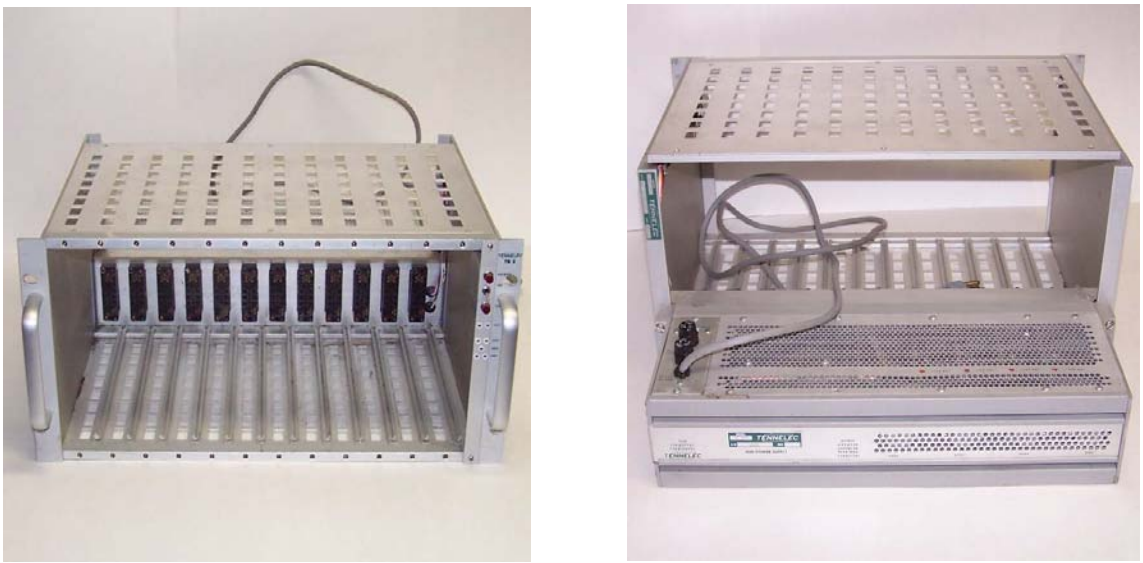


Figure 3.7: NIM BIN & Power Supply used in our setup

Standard Modules like discriminators, Fan-In-Fan-Out, Logic Units etc are designed and constructed to fit into the standard bins which supply the modules with standard power voltage Any NIM module will fit into any bin. By collecting the specific modules for a given application, an electronic system can be easily be created by installing them into NIM bins and cabling accordingly. Flexibility of the standard NIM's is that the modules can always be rearranged for any new experiment. Logic signals are usually exchanged between front panel, BNC or LEMO type connectors on 50 ohm coaxial cable at standard NIM label.

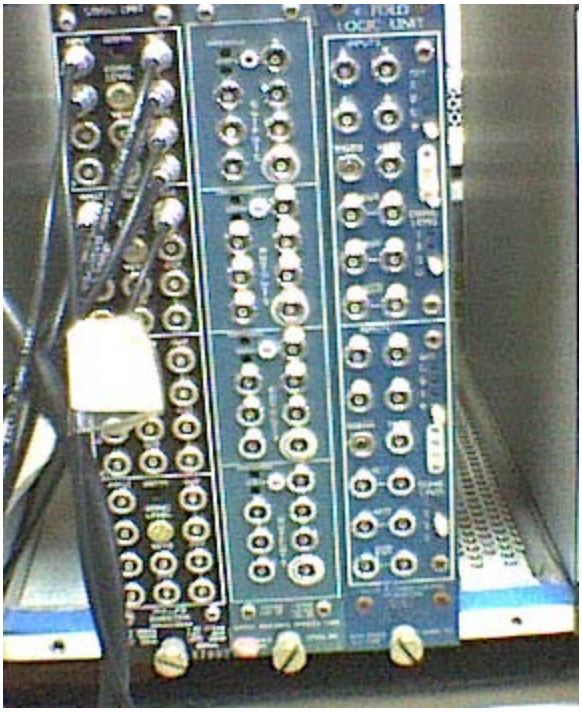


Figure 3.8 NIM Modules like discriminators, inserted in NIM BIN

NIM Standards specifies three sets of logic labels [1] [6] [7]:

- *Fast negative logic*: They are referred to NIM logic, employs fast signals with rise time on the order of 1ns and comparable width. This type of signal is being used in our setup where we have high count rates or fast timing. Fast logic signals are defined as current into 50 Ω load.

  Logic 1: -14 mA to -18 mA
  Logic 0: -1mA to + 1mA (+ 50mV or - 50 mV)

  The input and output impedance of all the fast modules is required to be 50 Ω.
  The corresponding voltage levels are 0V and -0.8V. For fast negative logic signals terminated cables with 50 Ω terminators are to be used because of fast rise time, to prevent reflections.

- *Slow positive logic:* They are referred to signals of relatively slow rise time, on the order of hundreds of nanoseconds or more. They of positive polarity. They are defined in terms of voltage across 1000 Ω impedance. This means that the current carried by the signal is very small. As per the NIM standards, signals are defined by following limits:

| | Output (must deliver) | Input (must respond to) |
|---|---|---|
| Logic 1 | + 4 to + 12 V | + 3 to+12 V |
| Logic 0 | + 1 to - 2 V | + 1.5 to – 2 V |

As for as the positive logic signals, following standards are further added to the NIM Standards:

Pulse width: normally 0.5 $\mu$ s

Source impedance: normally $\leq$ 10 Ω

Input impedance: normally $\geq$ 1000 Ω

Connections of the NIM Standard, positive logic sources and loads should be made with 93 -Ω coaxial cables. For length up to 1.5 m, impedance-matching cable termination is not required. A 100 Ω terminator at the receiving end is however required for longer cable lengths.

- *TTL and ECL voltage logic:* TTL (Transistor Transistor Logic) and ECL (Emitter Coupled Logic) is not a part of NIM Standard. However for the experimental high energy physics, TTL and ECL voltage logic systems are used in NIM modules.

| | TTL | ECL |
|---|---|---|
| Logic 1: | 2 - 5 V | - 1.75 V |
| Logic 0: | 0 - 0.8 V | - 0.90 V |

TTL is positive going logic which is often found in NIM Modules. ECL is the fastest form of digital logic. The levels are defined above. To make the ECL compatible with NIM standards, levels at both input and output are adopted. Another option is the use of ECL modules where we can directly enter the ECL levels. When we compare ECL with NIM logic, we find that the two standards are almost of same logic swing.

### 3.5.1 SIGNAL TRANSMISSION (CO-AXIAL CABLES):

Logic signals in our setup need to be exchanged from one module to the other or more specifically various modules are to be interconnected. Transmission of the signals should be done without loss of information contained. Pulses to be transmitted consist of continuous spectrum of frequencies, which means our interconnecting cables shall have to be capable of transmitting a wide range of frequencies uniformly over a desired distance. An ideal cable does not exist because of capacitance, inductance and resistance in any conductor causing attenuation during transmission and distortion at receiving end.

Fast pulses passing through a simple wire causes distortions just after few centimeters only. In high energy experiments we use co-axial cables to overcome the problem faced during transmission of signals from one end to the other.

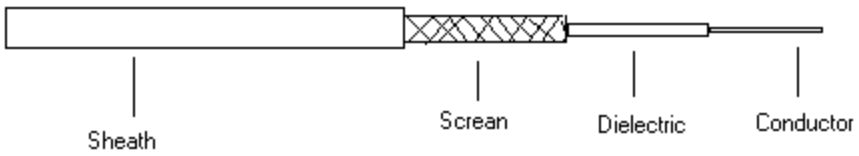



Figure 3.9: Construction of Co-axial Cable

Basically co-axial cables consists of two concentric cylindrical conductors separated by a dielectric material. Figure 3.9 shows the construction of a co-axial cable. The outer cylinder carries the return current which is made up of a wire mesh. The dielectric material is either polyethylene or teflon. The cable is protected by the outer covering. The outer cylinder not only serves a ground return but also as a shield to the centre wire from stray electromagnetic fields. For the fast electronic signal transmission in our set up we use RG- 174A/U (50 Ω). For the high voltage transmission we use RG 59/U (75 Ω). Lemo connectors are used for these coaxial cables for establishing a plug-in type connection on the front penal of each NIM and Camac module.

The co-axial cable because of the geometrical configuration, contain certain self capacitance and inductance. The cable also has some resistivity due to the fact that conductors are not perfect. Also there is some conductivity across the dielectric due to its imperfectness as an insulator. Because of the fact that cables contain capacitance, inductance and resistance, we can represent a unit cable as an equivalent circuit shown in the figure 3.10.

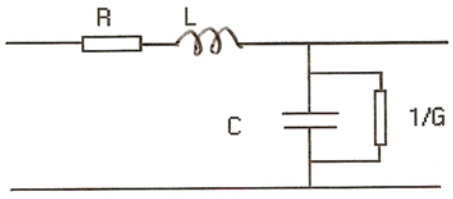



Figure 3.10: Equivalent circuit for length of a co-axial cable

L and C are, respectively, the series inductance and capacitance per unit length, while R is the resistance per unit length and G is the conductance of the dielectric which is presented here as parallel resistance of $1/G\,\Omega$. R and $1/G\,\Omega$ are the two quantities which are responsible for the signal loses. In case of an ideal cable R and G are Zero.

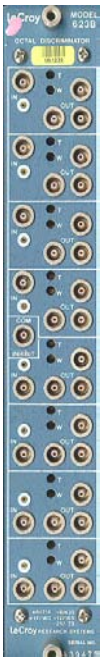
Presence of components as is clear from the figure 3.10 above in the equivalent circuit, cause signal delays across the length of the co-axial cable. The characteristic impedance of the coaxial cable in use of our experimental setup is $50\,\Omega$ and typical value for delay = 5 ns/m. The characteristic impedance can not be measured with normal resistive bridge but behaves as a real impedance when connected to an output of a device. It is in fact the impedance offered by the cable which causes propagation in the line. Signals in co-axial cables, in general is the sum of the original and reflected signal in the opposite direction. This causes distortions which can be avoided by matching the device impedance to the cable impedance. This problem is being overcome by fast NIM standards. The input and output impedance of the NIM Modules has been matched with the cable which is $50\,\Omega$. However at occasions the mismatch can not be avoided. For example when we want to view a signal on oscilloscope, direct entry of signals will result in a mismatch as its impedance is $1M\,\Omega$. In such case the cable need to be terminated with additional impedance of $50\,\Omega$ in parallel with the oscilloscope. The signals on the oscilloscope are then reflection free. Special terminators are available so as to fit into the cables.

## 3.6 ELECTRONICS FOR SIGNAL PROCESSING AND DATA ACQUISITION:

We shall now discuss basic functions of various standardized modules (NIM Modules), adopted by nuclear electronics for information processing of pulse signals. These modules are inserted into the NIM power bins and interconnected to each other from the front panel of each module to form a system for our application. Once basic function of each module is understood and the system is wired with the help of co-axial cables described earlier, we shall go further to understand and establish data acquisition and digital processing of the pulse signals with the help of Camac System (Refer to 3.7). All modules under discussion are commercially available. Depending upon the combination of several functions, different manufactures provide variable models of these modules having variable functions. Basic operation of these modules, however, is same. One should therefore consult the manual provided by the manufacturer to know about the details of the features and operation of any particular model. We shall therefore be discussing the specific models in use of our setup, at the end of each description.

Standard Camac Crate has a built-in, digital data bus to provide computer communication with the modules. So Camac Crate becomes the integral part of the data acquisition for processing and storing the data which is being manipulated by different NIM and Camac modules.

## 3.6.1 DISCRIMINATORS:



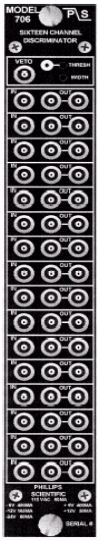
The function of the Discriminator is to accept the detector pulses and deliver a standard logic pulse. It is an interface between the real analog world of detector and digital world of logic system. The signals coming out of the PMT have significant low noise pulses present at their anodes. These low noise pulses need to be extracted out during the signal processing which is done with the help of "Discriminators". At its out put, the Discriminator delivers standard pulses related as closely as possible in time to the leading edge threshold crossings of the input signal. With the help of an adjustment screw provided at the front we can set threshold value in such a way that most of the low amplitude noise pulses are eliminated but signals pulses are not affected. The output pulses are of standard amplitude and duration, completely independent of all characteristics of the input signal except time of occurrence. The output of a discriminator is used as gate associated portions of the data collection system or generates pulses which are to be counted.

The Standard Discriminator Modules are available with variable feature like number of input and output channels, common or variable threshold voltage per channel, width control etc. Accordingly we are using the following Discriminator modules of M/S LeCroy and M/S Phillips:

1. <u>NIM Model 623B Octal Discriminator from LeCroy:</u>

It is eight channel discriminator featuring high sensitivity, high speed, and updating performance. Variable Threshold and Output Width can be set on each channel separately. Each channel has three outputs. Threshold voltage can be set between -30 V to -1 V via front panel screw adjustment for each channel. The measurement and setting of the threshold voltage can be done with the help of a voltmeter. The module has capability of updating which permits retriggering while an output from a previous input is still present. A second pulse, which exceeds threshold while an output is already occurring, extends the present output by the present width. However if the second threshold crossing occurs within the double pulse resolution time, the module will not respond. (Refer to Manufacturer's manual for more details and technical specifications ).

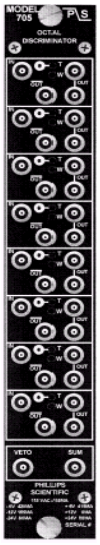
2. <u>Model 706, Leading Edge Discriminator from Phillips Scintific:</u>



It is a 16 Channel single Width NIM Module with common threshold and width controls. Threshold voltage can be set between -10mV to -1Volt via a 15 turn front panel control. There is provision of a test point on the front panel where we can set the desired threshold with the help of a Voltmeter Likewise the width can be set between 5nSec to 150nSec, with the help of another screw provided. The width once set shall remain of the same duration regardless of the input rate conditions. The outputs are current source type with one pair of negative bridged output per channel. When only one output is used, a double amplitude pulse shall be generated which is useful for driving long cables with narrow pulses. Two normal NIM levels are produced when both of the bridged outputs operate into 50Ω load. The output rise time and fall time is typically 1.5 n Sec, and their shapes are

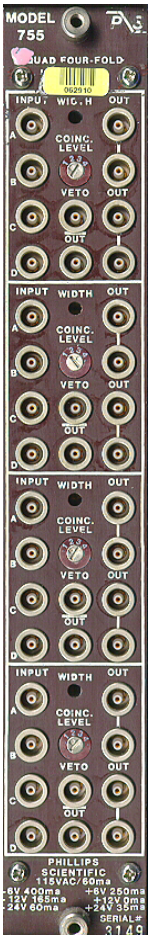
unaffected by loading conditions of the other outputs. (Refer to Manufacture's manual for more details and technical specifications).

3. Model 705, Octal Discriminator from Phillips Scintific:




It is an 8 Channel NIM Module with facility of setting independent threshold and width of each channel. In addition it a fast veto input and a summed output are common to all channels. Threshold can be set for each channel independently between -10 m V to -1 V with the help of provided test point providing a DC voltage ten times the actual threshold setting. Likewise each channel has an adjustable output width between 6 n Secs to 150 n Sec. The fast veto input allows simultaneous inhibiting of all channels to reject unwanted event early in the system. Similarly, a bin gate will inhibit the entire module when applied via the rear connector. In addition to a bridged pair of out put, a complimentary out is available. When one output of a bridged pair is used a double amplitude pulse is generated, when both the outputs are use a normal NIM level pulse is produced. (Refer to manufacturer's manual for more details and technical specifications)

## 3.6.2 FAST LOGIC UNIT & COINCIDENCE:




Fast Logic unit is used for coincidence label study of the signals of interest. For extracting out signals of choice from among pulses most of which could be noises or background, the coincidence technique is very useful. Coincidence of signals in time between two or more events served as powerful criterion for distinguishing signals from created noises etc. by the PMT. Though at discriminator label we are able to suppress noises by setting threshold voltage, yet it is difficult to suppress them completely. We can set the threshold value to some limit as otherwise we shall start loosing signals. The noises in PMT are random in nature. So it would be very rare that the noises are triggered in both, in coincidence.

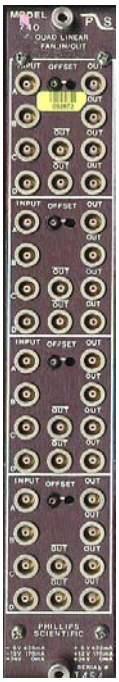
The logic unit is a coincidence module and performs logical "AND" operation. It is nothing but a logic gate. The output signal is "true" only if two or more logic signals are coincident in time. This way we are able to get pure signals from cosmic ray trigger.

**Model 755 Four Input Majority Logic Units from Phillips Scintific:**

This unit has four independent Channels of four input logic. That means each channel we can give four inputs and make a logic AND at the output. Each channel has four logic inputs, an anti-coincidence level switch and five outputs with common width control. Due to the versatility of the unit other logic functions like OR, Majority logic, Fan-In-Fan-out and anti coincidence function can be performed. The coincidence level switch provided at the front of the unit determines which logic function is needed at the output. The outputs are current

source type. The output pulse varies from 4nSec to 1 $\mu$ Sec which can be adjusted with the help of a screw driver. Width once set remains stable throughout. (Refer to manufacture's manual for detailed features and description.)

### 3.6.3 FAN-IN FAN-OUT:




Fan-Out module is distributes a fast signal to several parts of our Data Acquisition System with no loss of signal amplitude. The module divides the input pulses into several identical pulses of same height and shape. For generating energy spectrum we need to process the coincidence signal. The pulse from the counter under test is fanned out in two pulses. One is fed to the ADC for taking spectrum and the other is added to the two fold coincidence to get the three fold coincidence counts on the Scalar. The signal of the counter is also needed in our setup for taking TDC spectrum. Hence the module "Fan-In Fan-Out" plays an important role in our setup.

**Model 740 Quad Linear/Logic Fan-In-Fan-Out from Phillips Scintific:**

This Unit has four independent channels. Each channel has four linear or logic Fan-In of four inputs and Fan-out of six at the output. Four inputs allow summing of linear levels or pulses. Each channel has a DC offset control of $\pm 500$mVolts. (Refer to manufacturer's manual for detailed technical specifications and features).

### 3.6.4 SCALAR:

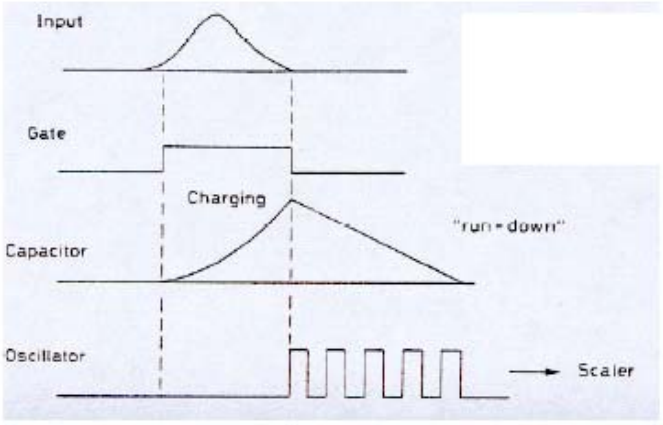

Scalar is a data acquisition module that can register logic pulses received during a given time period. We can use this module to either count pulses from the Discriminator or from the logic unit. With the help of this unit we can compare the counts of coincidence pulses with the counts of independent peddles. It is very useful unit for finding out the efficiency of the fabricated detector by comparing the counted pulses of two three or higher coincidences.

**Model 2551, 12 Channel Scalar from LeCroy:**

This model contains 12 identical 24-bit binary scalar. Each scalar is capable of responding to the NIM level logic signals of any duration down to 5 nsec. It accumulates any output signal generated by a discriminator or a logic circuit. Fast clear input enables fast rejection of unwanted data without data way operations. The scalar has a test mode facility to test all channels simultaneously without removing cables. It is a CAMAC standard module. The 24 bit data from any scalar is read in parallel to the common data way via rear card edge connector. Individual channel non-destructive readout is accomplished by generating a CAMAC Read and appropriate address. Using read and Clear channel will automatically be zeroed after reading the last channel. CAMAC clear will zero all the channels.

## 3.6.5 ANALOG TO DIGITAL CONVERTERS (ADC'S):

Analog signals must be digitized for data storage and subsequent analysis. The module ADC is used to do this job. It is a device which converts the information contained in an analog signal to an equivalent digital form Unlike discriminators, which simply indicate that an input was larger than some preset level, analog-to-digital converters give a quantitative measure of the size of the pulse. In high energy physics pulse parameters of interest is generally the total charge contained in the pulse, rather than peak amplitude. ADC'S are of two type: *peak sensing or charge sensing*. In peak sensing maximum of a voltage is digitized whereas in charge sensing the total integrated current is digitized. In case of photomultipliers in current mode, we use charge sensing ADC's.
The conversion technique employed in the ADC's used in our setup is 'Willkinson rundown' technique. The charge delivered to an integrating capacitor from the line gate is discharged at a constant rate. During the time this rundown is taking place, pulses from an oscillator are gated into the scalar resulting in the final count proportional to the charge originally stored by the capacitor.

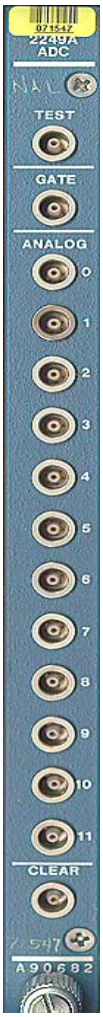



*Wilkinson method of analog-to digital conversion. The input is used to charge a capacitor which is than "run down" at a constant current. At the same time, a fixed frequency oscillator is gated on and the number of pulses generated during the time it takes the capacitor to discharge counted.*

Figure3.11: Willkinson method of Analog to Digital Conversion

Another method for conversion is Successive approximation method. Incoming pulses are compared to series of reference voltages to determine the height o the pulse. Because of the practical constrains of maintaining stable stored voltage levels this method is not adopted.

**12 Channel A-to-D Converter, CAMAC Model 2249 A from LeCroy:**




The model 2249 A contains 12 complete ADC's in a single-width module. Its special features are that it has expanded resolution, high sensitivity, stability, fast digitizing rate, LAM and Q suppression, provision of fast clear and calibrating test mode. It is a charge sensitive device and the Willkinson charge rundown technique is used in this module. The input sensitivity of the model is 0.25 pC/count for a full scale range of 256 pC. This model offers excellent event rate capability through the incorporation of fast clear and digitizing rate. The fast clear input enables the ADC's to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic. End of conversion of the module which contains data is flagged by generation of a CAMAC LAM.

## 3.6.6 TIME TO DIGITAL CONVERTERS (TDC)

Time to digital converters are modules used for fast time intervals in large variety. Time measurement typically involve the use of a pulse discriminator and time to digital converters TDC. Electronic time interval measurement involves digitizing the time between the two or more pulses. The first pulse is called START pulse and the later called STOP. A single input is used against which INDIVIDUAL inputs are timed. A MULTIHIT digitizer accepts a COMON input, then digitizes several INDIVIDUAL pulses which arrive at the same cable.

**High precision time to digital converter Model 2228 from Le Croy:**


The Le Croy model 2228A is a single width Camac module. It is Octal time digitizer . That means it has 8 independent channels, each of which measure the time from leading edge of a common Start pulse. Each channel disregards any STOP pulse received before a START signal and will accept only one STOP for every START. Conversion begins upon receipt of the START signal and proceeds until one of the following: a STOP signal is received; the cycle is terminated by application of the front panel CLEAR signal; or the digitizer reaches full scale.

This module converts the measured time intervals into 11 bit digital number using a 20 MHz internal clock for full scale digitizing time of 100 $\mu$ sec. The conversion clock is started in phase with the TDC start signal to ensure synchronization and eliminate the inaccuracy introduced by the free running oscillators.

Online testing is facilitated by either a front panel COMMON STOP input or by CAMAC command. A signal at COMMON STOP generates simultaneous stop for each channel, permitting accurate testing of he module.

The time to digital converter is one of the simplest timing instrument to set up and operate. The input signals are provided direct from the discriminators with no critical adjustments of amplitude or width being required. As soon as a stop pulse is received, the TDC begins an interval cycle which digitizes the time measurement output is available on command typically less than 100 $\mu$ sec after receipt of the start signal.
The TDC is used in our setup to measure critical time of flight to measure the PM pulse height, permitting slewing corrections to be made later.

## 3.7 CAMAC BINS:

Figure 3.12: Camac Crate from Kinetics with various Modules fitted in

CAMAC is an acronym for Computer Automated Measurement and Control. It is a modular data acquisition system used at almost every Nuclear and High Energy Physics research laboratory. It represents the joint specifications of US and European Committee. Thousands of scientific, industrial, aerospace and defense users have adopted CAMAC as a standard for their data acquisition and control projects. The primary application of CAMAC is data acquisition but it can be used for remotely programmable trigger and logic applications. The CAMAC covers electrical and physical specifications for the modules, instrument housing or crates and crate back plan. CRATES contain 12 positions or 25 positions. Back plan DATA WAN can support 16 bit or 24 bit wide DATA and transfers at a speed up to 1 million words/sec. Camac crates are individually controlled by slaves or intelligent controller. The Controllers are tied together with parallel branch highway that ends in branch driver. The branch drivers are interfaced directly to a data acquisition computer. Branch highway speed is 1 million 24 bit word/sec. A camac crate from M/S Kinetics is in use with our data acquisition system and is shown in figure 3.12.

## 3.7.1 CAMAC MODULS:

The basic building block of CAMAC system is modules, which is generally the interface between the external process and CAMAC internal bus called Data way. A wide variety of I/O modules is available, including discrete input and output, analog input and output, counters, controllers, transient recorders. Motor controllers, communication interface, memory buffers, and microprocessors. The modules we are using in the lab are ADC, TDC, Scalar and HV Power Supply.
The CAMAC standard (IEEE 583) specifies all the physical dimensions of modules, its power connections, Data way signal levels, command response protocol, and Data way cycle timing. Within these specifications, one is then free to implement any desired feature of the module. Input/output connections are made via connections on the front panel or in the rear I/O access area above Data way connectors. Many modules contain LED's, switches and test points for system diagnosis. The important feature of the CAMAC Modules is:

- They permit expansion and flexibility.
- The electronic data acquisition and/or control system can grow and evolve to match the demand of the application
- System can be reconfigured after the end of the experiment for the use in new experiment
- Higher bandwidth interfaces and pre-processors may be selected to match the application
- They are the electronic solutions for to days rapidly evolving environment.

## 3.7.2 THE CRATE CONTROLLER:

The crate controller generally resides in the right hand slot of the crate. It provides the hardware link between the I/O modules and computer. This acts as a communication centre managing the flow of information on the crate data way. Commands or data issued by a computer to a module or vice versa, must therefore pass through the crate controller. The crate controller addresses the modules with the appropriate CAMAC commands, transfer data, accept status information and monitor the interrupt lines, all via the data way. In general, within a given crate, the crate controller is the only module which can issue commands and thus the master of data way. All other modules are slaves to the crate controller.

### 3.7.3 COMPUTER INTERFACE:

Because CAMAC is a Computer independent, it can be interfaced to practically any computer with direct computer bus approach, where the crate controller is interfaced to the computer's peripheral bus. For recording the data of the Cosmic Ray Setup we have interfaced the CAMAC System to IBM PC/AT. A 16-bit IBM PC/AT Interface model 2927 from KINETICS is being used for the purpose. It is a computer bus adopter and is being mounted in the 16 bit ISA slot of the PC. The Interface is directly attached to the crate controller via 40-conductor twisted-pair ribbon cable. The CAMAC Hardware is provided with a software package including CAMAC drivers which is installed in the attached PC. ( Refer to the manufacturer's manual for features and more details)

### 3.7.4 DATAWAY COMMUNICATION:

All slots consists of a series of parallel wires running along the back plane .All the communications between the modules, crate controller and the host computer is made via these lines. Each slot provides power and all signals for crate controller and I/O modules. Modules are addressed via individual slot number (N) lines by the crate controller and receive commands in the form of a function Code (F) and Subaddress (A). The one microsecond timing cycle contains two timing strobes, S1 and S2, to clock the 24 bit Read or Write data into the module or crate controller. Two status bits indicate the validity of the data returned and command acceptance by module. A module can also initiate a service request interrupt (L), referred to as a LAM or Look At Me.

## 3.8 PULSE PROCESSING AND DATA ACQUSITION:

The electronic setup for pulse processing is shown schematically in the block diagram chapter 1.Two paddles are placed one upon the other at some distance and particle is allowed to pass through both. After discriminating the signals independently, the two signals are fed to the logic unit. If the particle triggers both the scintillators the signal in both PMT's would be time coincident. The output logic signal from the logic unit produces a 2-fold logic. This 2-fold output is formed only when signal (muon signal) is accepted by both master peddles which becomes gate to ADC (used to convert analog signals to digital signals). We can test any counter with the help of this gate by placing any test counter in between the two master peddles. The signal from the test counter is fed to ADC and TDC for spectrum study of 2- fold and 3-fold logic via FAN IN FAN OUT where signal get divided with same height and shape. The gated ADC with the help of 2-fold logic receives direct analog signal from the test counter PMT at its input where as for TDC the 2-fold is used as start and the discriminated output as stop logic. ADC and TDC outputs give data way to the computer automated measurement and control standard (CAMAC) which are further fed on to the computer by CAMAC Controller and Interface (Installed in the PC).On PC we get the desired ADC and TDC Data of the charged particle.

For checking the efficiency of a counter under test we have a Scalar Unit with which we can have counts from each paddle, 2-Fold counts and three fold counts. In our setup e.g. we get the counts of each peddle on channel 0 and 1, the 2-fold counts on channel 3 and 3-fold counts on channel 4. Since the scalar has no display of its own, we see the counts on to the PC by opening the corresponding program. This way we can let the experiment go on for hours together and let it be stored by the PC in a data file. For finding out the efficiency of the counter, we simply divide the counts of 3-fold counts with 2-fold counts.

$$\text{Efficiency } (\eta) = \frac{\text{No. of counts of 3-fold}}{\text{No. of counts of 2-fold}}$$

Unlike discriminators, which simply indicate that an input signal was larger than some preset label, analog to digital converters (ADC'S) give a quantitative measure of the size of a pulse. In particle physics, the pulse parameters of interest is generally the total charge contained in the pulse, rather than its peak amplitude. So we shall be using current integrating (Charge) ADC. This device integrates an input current for a duration of time equal to the width of an applied gate signal and performs an analog to digital conversion on resulting charge. The two fold coincidence is therefore fed to the ADC gate and the charge signal i.e. the analog signal (detector signal) is fed to the input of the ADC module. In our case we are directly taking the detector signal from the PMT. Charge ADC sensitivity is expressed in pC.
The two fold coincidence signal works as high speed linear gate to ADC, which opens and closes in few nanoseconds. This permits the selection in time of the pulse from the detector to be analyzed. The linear gate completely blocks all inputs while it is closed and when open, passes all inputs without distortions. ADC measure the charge and produce a digital number proportional to the input signal. The converted digital signals are given out by the ADC to the PC via camac data way.
We shall now divide the total setup into small systems for performing simple experiments thereby understanding various techniques for pulse height selection and coincidence techniques.

## 3.8.1 SIMPLE COUNTING SYSTEM:

We get signals from scintillation detectors which are to be counted. Figure 3.14 shows the schematic diagram of the modules and connections necessary in setting up of such a system needed for counting of signals from the detector.

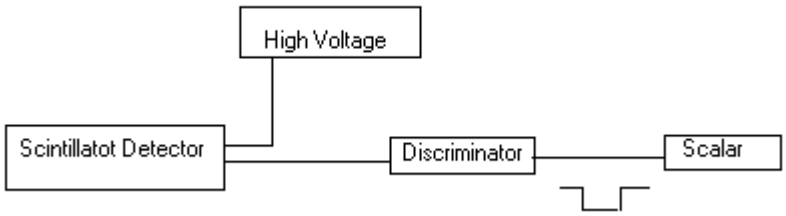



Figure 3.14 : Simple Counting System

In this setup analog signal from the detector is directly fed to the discriminator which delivers a standard logic NIM signal for every analog signal higher than the threshold. The logic signal is then sent to the scalar which counts each arriving signal. Care is to be taken that both scalar and the discriminator is of correct logic type i. e. it accepts positive or negative signal. In our case since we have negative logic signals coming from the detector, we have both the modules which accept negative logics.
The discriminator in our setup serves two purposes. One is it excludes low level noises and the second is it gives shape to the accepted signal to form acceptable signal to the scalar. This is done by adjusting the threshold voltage at the discriminator. Threshold is to be adjusted to ensure that noises are eliminated, but it is not be adjusted so high as to cut out the signal. With the help of oscilloscope we observe the signal directly from the detector and find out the noise level first and then accordingly set the threshold voltage of the discriminator.
Scalar module is to be selected according to the count rate desired. Accordingly the units are selected as per the schematic details.

## 3.8.2 THE SYSTEM FOR THE COINCIDENCE TECHNIQUE:

The electronic determination of the particle going through two or more detectors in coincidence is represented in the schematic diagram in figure 3.15. Like pulse height selection, coinciding in time between two or more events serves a powerful criterion for distinguishing reactions.

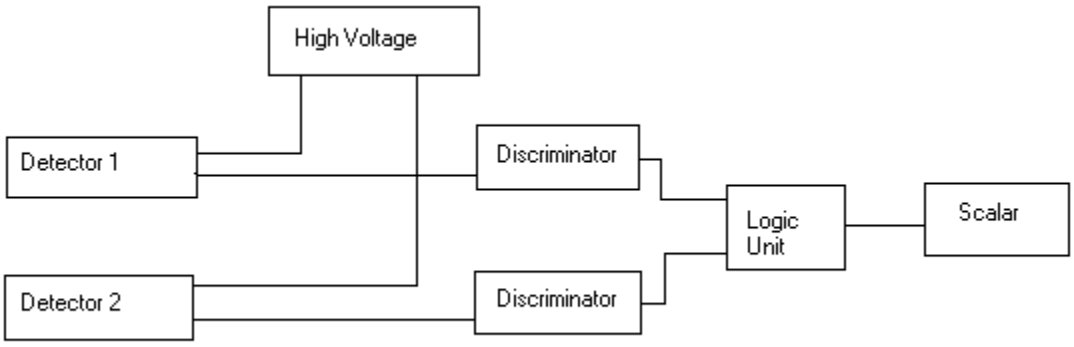



Figure3.15: A system for coincidence measurements

The basic principal of the coincidence technique is that we convert the analog signals from the detectors into logic signals and then send them to a coincidence unit called *logic unit.* The functioning of this logic unit is described in previous chapter. If the two signals are in fact coincidence the logic unit gives an output.

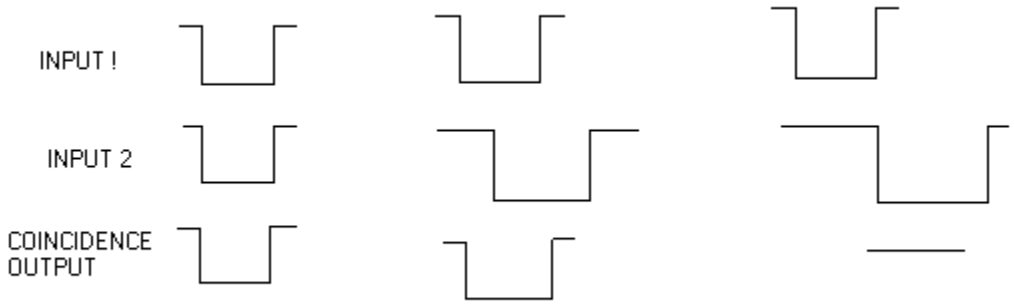



Figure 3.16 Coincidence between pulses

Figure 3.16 shows some examples of coincidence and non coincidence pulses. A coincidence is produced if any part of the two incoming signals, overlap. This happens in an ideal case. However in reality a minimum overlap is needed before it can be recognized as coincidence. All pulses arriving within a time equal to the sum of their width are registered as coincidence.

It is very important in this set-up that all cables of each branch leading to the coincidence module are of the same length. It is therefore necessary to ensure that the cables are fabricated after calculation of delays.

### 3.8.3 SYSTEM FOR COUNTER EFFEICIENCY:

The system for testing a fabricated scintillation counter and finding its efficiency is shown in figure 3.17.

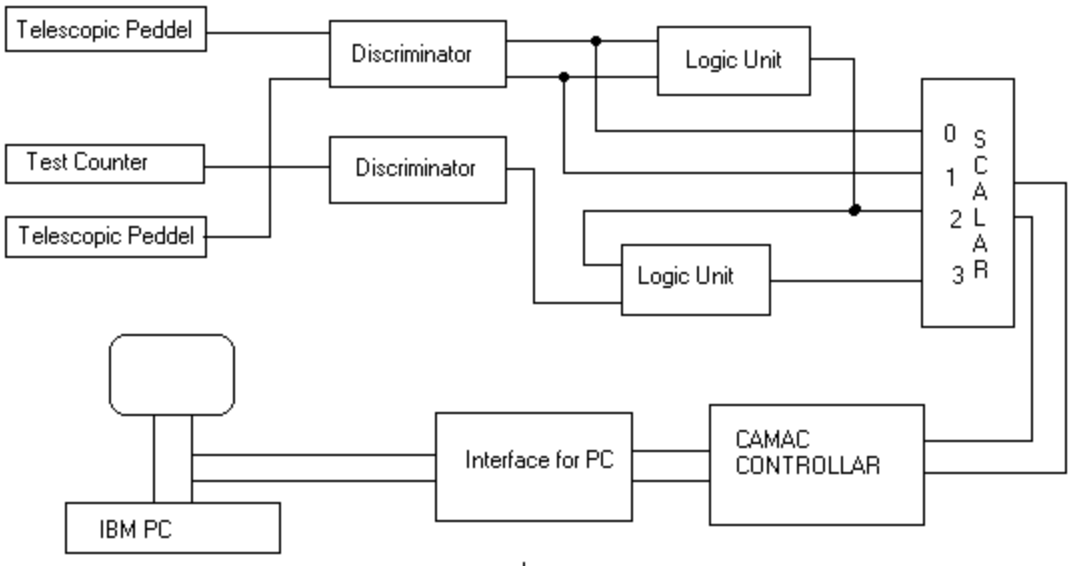



Figure3.17: The System for counter efficiency

The counter under test is placed between the two master paddles and cosmic muons are allowed to pass through all the three. The geometrical arrangement of the two master peddles and the counter is so done that surface area of the three overlaps each other. This is important to have maximum number of counts in coincidence. The counter under test is given the required high voltage and the signal is observed on the oscilloscope for its height, amplitude and noises etc. After studying the signal on oscilloscope we know the threshold voltage to be set at the discriminator channel to which the counter signal is to be attached for discriminating and converting into NIM signals at the output. The two signals from the master peddles are fed to the logic unit after discriminating independently. If the particle triggers both the scintillators the signal in both the photomultipliers shall be time coincident. We get 2-fold coincidence at the output of the logic unit. This two fold output is formed only when signal is accepted by both the master peddles. This 2-fold signal is now fed to another input channel of the logic unit. Similarly the signal from the counter is also fed to the same channel of the logic unit where the 2-fold signal is fed. The output of this logic unit channel then gives us the 3-fold coincidence.

For checking the efficiency of the counter under test we have a scalar module for counting 2-fold and 3-fold counts. In our system we connect the independent counts of the two master peddles to channel 0 and 1 and 2-fold, 3-fold counts to the channel 2 and 3 of the scalar unit respectively. Since Scalar has no display of its own and is a camac module, it is wired to a computer through camac controller and PC interface. A simple software is provided in the PC with which help we can have reading of each channel of the scalar. The efficiency of the counter under test is calculated by dividing the 3-fold counts to the 2-fold counts.

$$\text{Efficiency } (\eta) = \frac{Number\ of\ counts\ of\ 3-fold}{Number\ of\ counts\ of\ 2-fold}$$

OBSERVATIONS:

The top and the bottom peddles are standard peddles with EMI photomultiplier numbers 66264 and 66272 respectively. The third photomultiplier tube number 66265 is used for the test counter X. The optimum operating voltage for all the tubes is given as HV = 1550V. The threshold voltage all the three counters is 40mV. The following tables gives the record of reading taken on the scalar and the calculated efficiency of the counter X.

TABLE 1

Rate/10 minute:

| CHANNEL | COUNTS | FREQUENCY |
|---|---|---|
| 0 (Peddle A) | 21553 | 35.9 |
| 1 (Peddle B) | 19279 | 32.1 |
| 2 (2-fold Coincidence counts) | 523 | 0.9 |
| 3 (3-fold Coincidence) | 507 | 0.8 |

Efficiency of the counter X is 96.94%

TABLE 2

Rare/10 minutes:

| CHANNEL | COUNTS | FREQUENCY |
|---|---|---|
| 0 (Peddle A) | 22434 | 36.2 |
| 1 (peddle B) | 20171 | 33.5 |
| 2 (2-fold Coincidence Counts) | 519 | 0.9 |
| 3 (3-fold Coincidence Counts) | 504 | 0.8 |

Efficiency of the Counter X is 97.10%

TABLE 3

Rate/10 minutes:

| CHANNEL | COUNTS | FREQUENCY |
|---|---|---|
| 0 (Peddle A) | 22628 | 36.0 |
| 1 (Peddle B) | 20752 | 32.9 |
| 2 (2-fold Coincidence Counts) | 514 | 0.9 |
| 3 (3-fold Coincidence Counts) | 498 | 0.8 |

Efficiency of the Counter X is 96.88%

The above three tables are the repetition of the reading taken on Counter X. We normally let the counter test for more time and take repeated readings. The average efficiency of the readings given in three tables of counter X comes out to be above 96%.

## *CHAPTER 4:*

## *SCINTILLATION TILES USING WLS (WAVE LENGHTH SHIFTING) FIBER FOR LIGHT COLLECTION:*

Experimental High Energy Physics (EHEP) group at Panjab University fabricated scintillation tiles for HO (Hadron Outer Calorimeter) in CMS (Compact Muon Solenoid) experiment at CERN. HO detector is array of scintilator tiles forming a tray. Figure 4.1 and 4.2 shows the top view and cross section of a typical HO Scintillation tile to be fabricated. Wave length shifting (WLS) optical fiber embedded in these tiles is used as light collectors to be coupled to clear fibers (of negligible attenuation length), which will run several hundred meters to be interfaced to the electronics readout via Hybrid Photo Diode ( HPD's). WLS fibers are held inside the tile in groves with keyhole cross section. Each groove has a circular part (of diameter 1.35-mm) inside the scintillator and a neck of 0.838-mm width. The groove is 2.105 mm deep. Four identical grooves are made in each quadrant of the tile. The corners of the groove are rounded to prevent damage to the fiber at the bend and to ease fiber insertion. Entry point of the fiber is specially designed to for each insertion. These tiles are further assembled together to make a tray for HO detector using plastic tray covers. The sides of the tiles are painted with white Bicron paint for better light collection. Grooves and holes are done on CNC milling machine. Special Straight cutters and ball cutters are used to establish the groove inside the tile. Scintillator material BC 404 from Bicron is being used to make tiles. Thickness of the material is 10 mm. The detailed fabrication procedures are well described in, "Fabrication of Scintillation Tiles" by V.K.Bhandari, available in the EHEP lab [8].

The tile is the smallest unit of HO, which is the integral part of each ring of the detector e.g. +1 or -1 and so on. Each ring is divided into 12 identical sectors. Each sector has 6 trays and each tray has six tiles for ring +1 and -1. One sector is made up of 6X6=36 tiles. A total of 12 sectors constitute a ring i.e. each ring is made up of 36X12=432 tiles. So EHEP group of PU fabricated tiles for complete two rings i.e. ring +1 and ring -1. Multiples of Tiles of 36 different dimensions were therefore made to fulfill the final target of completing tiles for both the rings.

Tiles were further assembled into trays. Six tiles were put together between the two plastic covers which were suitably packed in tyvec and tedler paper. The required fibers were fabricated in the shape of pigtails and further inserted inside each groove of tile. All the fibers coming out of the tray were mounted into a connector which is then fixed on the side of each tray for further connecting to the readout electronics etc. These trays were then tested with the help of X -Y Scanner before sending to CERN for final Installation.

Light emission from the tile is in the blue-violet, with wavelength in the range $\lambda$ = 410 – 425 nm. This light is absorbed by the waves shifting fibers with fluoresce in the green at $\lambda$ = 490 nm. The green wave shifted light is conveyed via clear fibers waveguide to connectors at the end of tiles. [9]

Signals are collected from the end of the tiles via optical cables. These signals are then transferred via fiber optic wavelength bundles to readout boxes that collect, decode, and electronically amplify the scintillation signals from the tiles. The readout boxes convert the scintillation signals from the "layer" geometry of the tiles to the "tower" geometry which is appropriate for energy measurement. This means that individual tiles which sit one-behind-another in depth are optically added together so that energy within a given zone, called a tower, is determined. This technique is used for the readout of HB, HE and HO detectors in CMS experiment.

The devices which detects the optical signals and convert them to electrical signals are photo sensors called hybrid photodiodes ( HPD's).

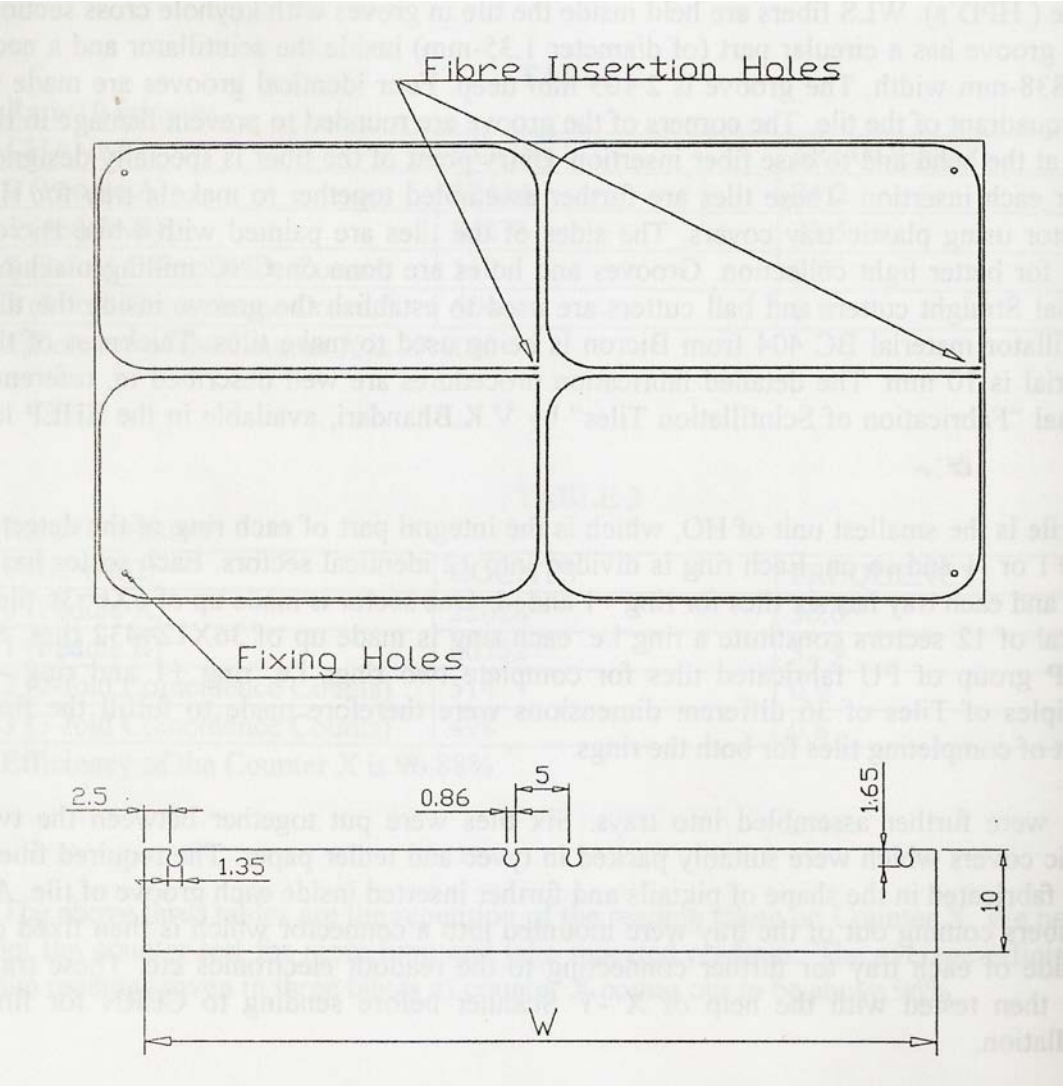



Figure 4.1: Design of a typical tile. Four σ grooves and four holes are seen. Bottom drawing shows the cross-section of a tile showing the grooves dimensions.

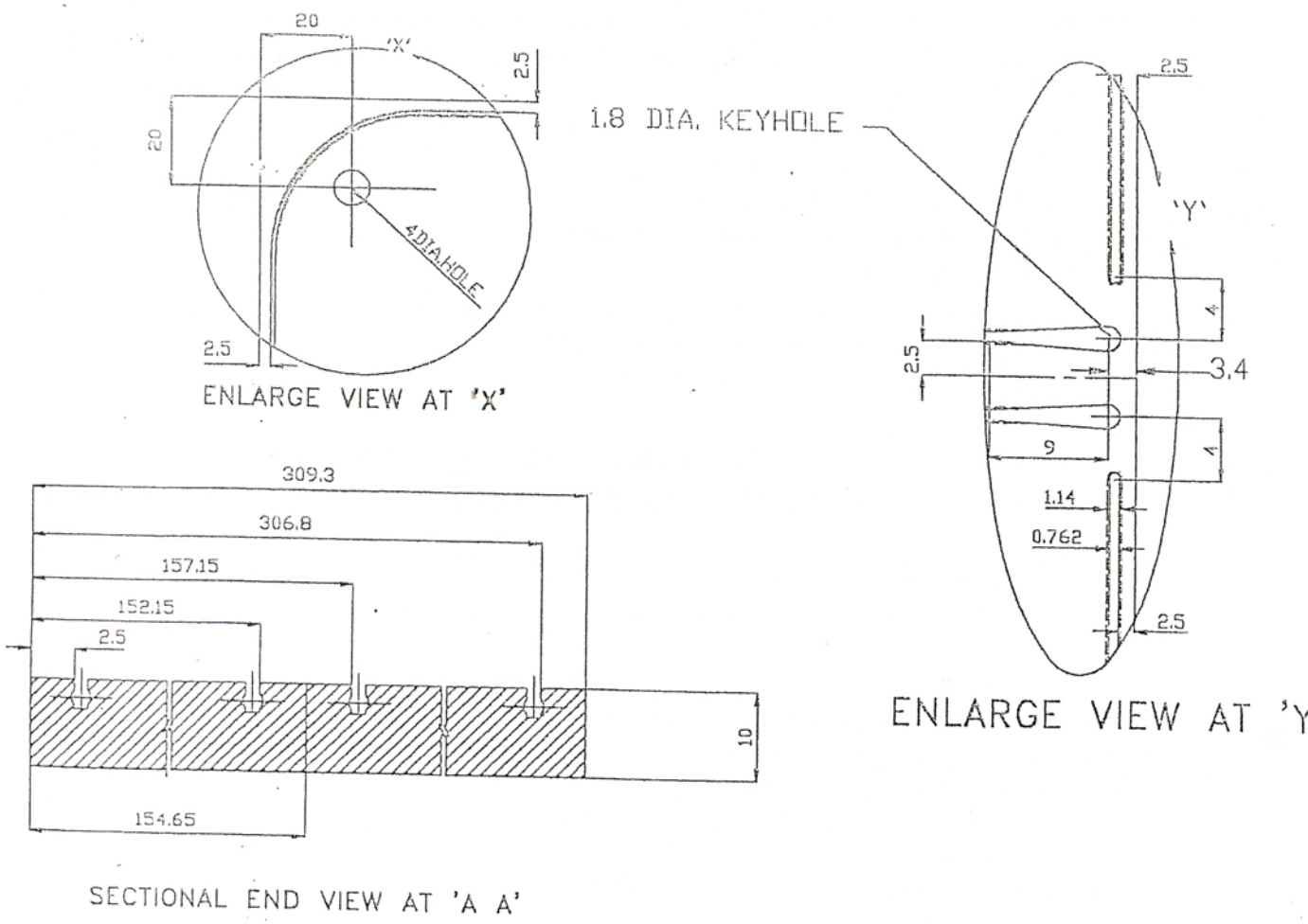



Figure 4.2: View at X and Y of the drawing in figure 4.1

## 4.1 TESTING OF PLASTIC SCINTILLATION TILES FOR EFFICIENCY:

The efficiency of the scintillation tile is number of photo electrons that the Photomultiplier emits, when for example muon passes through the tile.
Following factors decide the overall efficiency of the fabricated scintillation tile:

- The efficiency of the plastic scintillation material used for converting the energy deposited into photons.
- The number of the fibers used to collect photons.
- How well fibers are fixed in the tile?
- How well the fibers-tips are polished?
- How well the tile is wrapped up and with what?
- Attenuation length of the fiber
- Quantum Efficiency of the PMT: incident photons must be of the same wavelength as specified by the manufacturer of PMT.
- Cleanliness while handling/wrapping the tile

### 4.1.1 ASSEMBLY OF SCINTILLATION TILE AS A MODULE:

### 4.1.1.1 MATERIAL & COMPONENTS REQUIRED:

1. The grooved Scitillation tile
2. Cookie (round) cut into size of PMT with hole in the centre for inserting four fibers
3. Optical Glue Bicron 600
4. White reflecting paper (Tyvek) for wrapping
5. Black paper (tedler) for second wrapping
6. Photomultiplier Tube (PMT) 9807B (Pre Calibrated)
7. Voltage divider for PMT EMI 9807B
8. Aluminium housing for PMT
9. Aluminium housing for voltage devider of PMT
10. Fixed Lemo Socket ERA 00.250CTL
11. HV Connector/Socket (MHV Type)
12. Co-axial cableCCE.99.298.505 (For LEMO)
13. Silicon Greece
14. Aluminium foil tape
15. Four WLS fiber of the required length
16. Hand gloves, tissue paper, cotton cloth and methylated alcohol

### 4.1.1.2 PACKING OF TILE MODULE:

Figure 4.3: A Scintillation Tile with embedded grooves

Following steps illustrate how to practically pack and attach the single tile to photomultiplier for study of the signal and finding the efficiency:

Step 1:

Keep the material mentioned above ready.

Step 2:

Clean the tile with methylated alcohol. Also check the grooves for any material left inside while machining. Use hand gloves while handling the tile

Step 3:

Cut tyvec paper to the required size for first packing. Mark the entry of the grooves on the cut paper and wrap the tile in tyvec by using silver foil. See that the entry holes of each groove match with the marking while packing. Make the hole on the marking with the help of a sharp cutter.

Step 4:

Repeat step 3 by using black tedler paper.

Step 5:

Insert fiber into the grooves one by one in such a way that it covers the whole groove.

Step 6:

Now take the cookie and insert the other end of all the four fibers in the hole.

Step 7:

Now prepare the optical glue by mixing the two components i.e. 5gm of resin and 1.5 gm of hardener

Step 8:

Apply the mixed glue to the fibers at the hole for fixing the fibers in the centre of the cookie. Let 2-3 cm of the fibers come out the cookie while applying glue. Keep the tile aside for some hours after applying glue.

Step 9:

Assemble the voltage divider using Lemo Socket and HV Socket with the help of aluminium housing provided for it. Solder the HV wire and signal wire with respective sockets.

Step10:

Plug in the Photomultiplier to the voltage divider socket. Apply some optical grease to the face of the Photomultiplier.

Step 11:

Cut the extra fiber coming out of the cookie and polish the face of the four fibers.

Step 12:

Attach the cookie to the face of the Photomultiplier with the help of the Aluminium coupling provided. Use black tape to attach the cookie and the Photomultiplier assembly.

The assemble tile as test module is shown in figure 4.4

Figure 4.4: The assembled tile as module for testing

## 4.2 TESTING OF TILES:

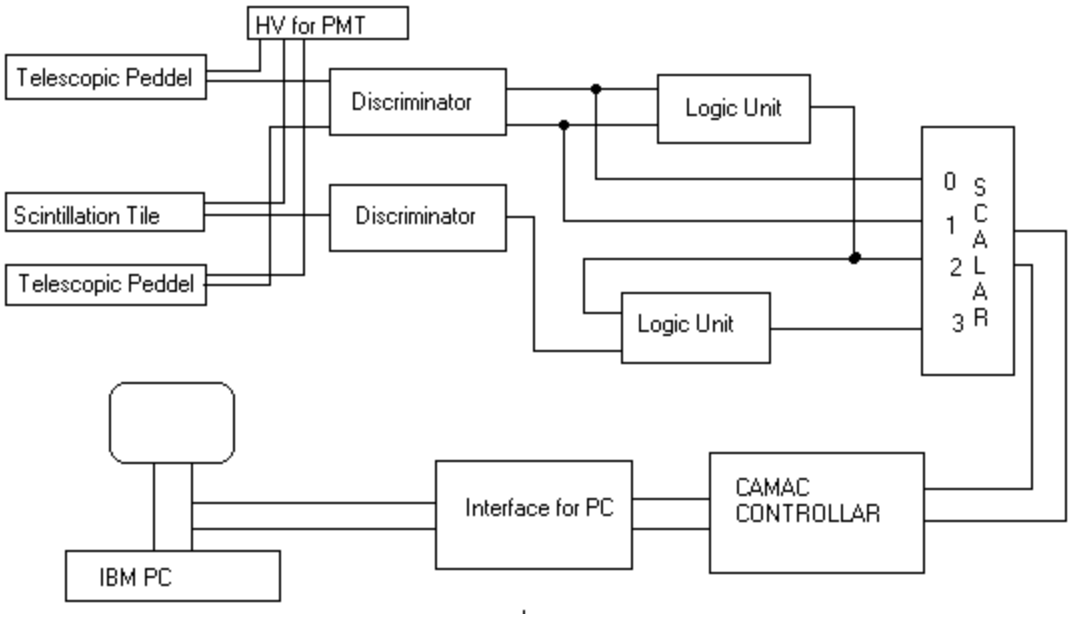



Figure 4.5: The cosmic ray set-up and data acquisition for testing of tile

We shall be testing our tile as single module with the help of the cosmic ray setup and data acquisition system described in chapter 3. The block diagram of the system used to test the tile module is given in figure 3.5. The assembled tile module is kept in between the two master peddles for signal study as well as finding out the efficiency by using cosmic muons as trigger. We will first study the signal on oscilloscope by giving suitable operating voltage to the photomultiplier (PMT). A well formed signal should be observed if the tile module is assembled properly and with full care. After satisfactory study of the signal on oscilloscope, we shall check the tile in coincidence with the two master peddles. Since we are testing the tile as single module, which has only four fibres, signals observed on oscilloscope are weaker than the signals coming out of the two master paddles. So the signals from the tile module are to be handled separately as compared to the signals from the two peddles. The signals are of the low amplitude and low noises. So the signal need to be processed by a separate discriminator where different valued threshold need to be set.

Two fold signal as described earlier is taken and fed to the Scalar after discriminating the independent signals of the two peddles and then adding them with the help of Logic unit. Simultaneously the signal from the tile module is fed to the Scalar after discriminating and adding to the two fold signal from the peddles. Two fold and three fold coincidence counts from the logic unit are fed to separate independent channels of the scalar module which is a camac module. As we know the camac modules are interfaced to a PC via camac controller through a data bus, the counts are directly read at the PC by opening the scalar software file. Counts are taken of this tile as three fold coincidence and compared with the two fold to check the tile for its efficiency as follows:

$$\text{Efficiency } (\eta): = \frac{Counts\, of\ two\ fold\ coincidence}{Counts\, of\ three\ fold\ coincidence}$$

We let the experiment go for a good length of time say two to three hours and repeat the same twice. In this way we test each tile after suitably assembling each and get to know the efficiency of each tile before the tiles are further assembled into trays for testing and then finally installing in the CMS detector at CERN.

## 4.3 INTRODUCTION TO FIBER OPTICS [10] [11]:

Fiber-optics is an appropriate means of communication. It is a similar system to the copper wire system that the fiber-optics is replacing. The difference is that the fiber optics use light pulses to transmit information down fiber lines instead of using electronics pulses to transmit information down copper lines. A basic fiber optics system consists of a transmitting device, which generates the light signal, an optical cable, which carries the light and a receiver, which receives the light signal.

The transmitter accepts the coded electronic pulse information coming from copper wire. It then processes and translates the information into equivalently coded light pulses. A light emitting diode (LED) can be used for generating the light pulses. Using a lens, the light pulses can be funneled into the fiber-optics medium where they transmit themselves down the line.

Pulses are transmitted in fiber optics because of the principal known as total internal reflection. "The principle states that when the angel of incidence exceeds a critical value, light cannot get out of the glass, instead, the light bounces back in." This principle is applied while constructing fiber optic strand, and thus information is transmitted down fiber lines in form of light pulses.

There are five elements that make-up the construction of a fiber strand, or cable (figure 4.6 ):

- The optical core
- Optical cladding
- A buffer material
- A strength material
- The outer jacket

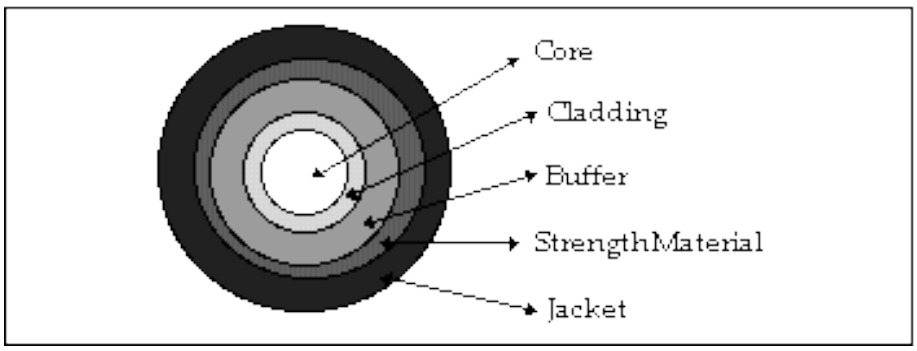



Figure 4.6: Cut away of a fiber-optic cable

The optical core is the light carrying element and centre of the optical fiber. It is commonly made up of silica germania. The optical cladding is surrounding the core and

is made up of pure silica. It is his combination which makes the total internal reflection possible. The difference in material used in the making of core and cladding creates an extremely reflective surface at the point in which it interfaces. Light pulses entering the fiber core reflect off the core/cladding and thus remain within the core as they move down the line.

The buffer material, help shield the core and cladding from damage. A strength material surrounds the buffer, preventing problems when the fiber cable is being pulled. The outer jacket is added to help against abrasion, solvent and other contaminants.

Once the light pulses reach their destination they are channeled into the optical receiver.

## 4.3.1 PRINCIPLE:

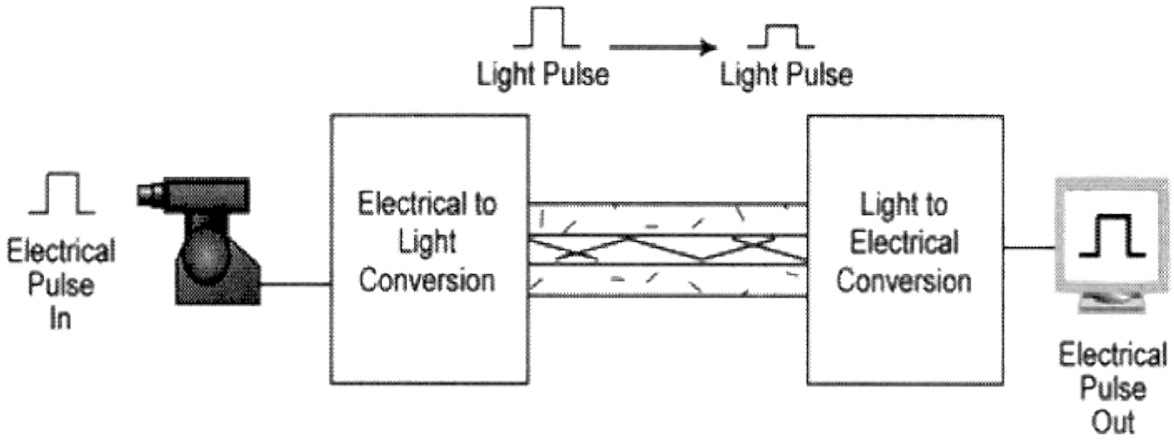



Figure 4.6: Transmission principle of the signals via fiber optics

Figure 4.6 represents the principle as to how the electrical pulses are transmitted through optical fibers. Electrical pulses are first converted into light pulses and light pulses are transmitted through the optical fibers and again converted into electrical signals for further use and processing.

Fiber optic transmission uses the same basic elements as copper based transmission systems:

- A transmitter
- A receiver and
- A medium by which the signal is passed from one to other

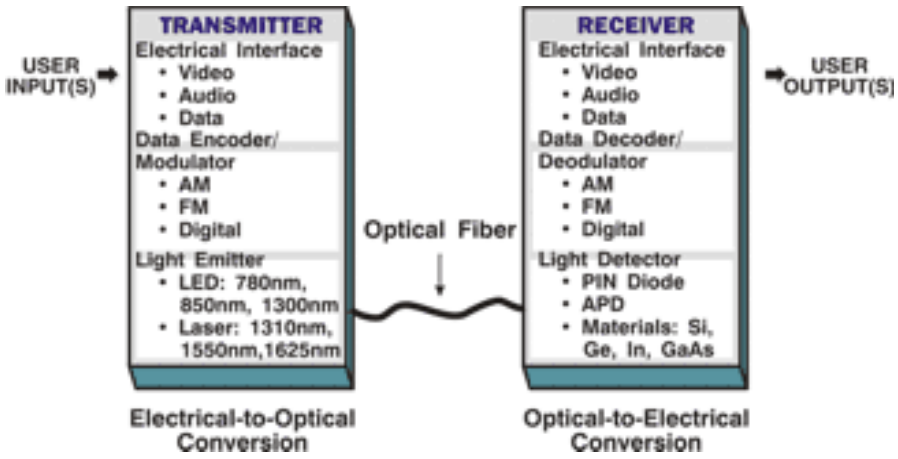



Figure 4.7 Elements of a Fiber Optic Links

The transmitter uses an electrical interface to encode the information through AM, FM or digital modulation. A laser diode or LED do the encoding to allow an optical output of 850 nm, 1310 nm, or 1550 nm (typically) [11]. The optical fiber connects the transmitter and the receiver.

At the receiving end there is either a PIN photodiode or an APD to receive the optical signals and convert them to electrical signals.

## 4.3.2 OPTICAL FIBER PARAMETRS [12]:

**Wavelength:**

The light which can be seen by the human eye is said to be in the visible spectrum. In the visible spectrum, *wavelength* can be described as color of light.

We notice from the figure 4.8 that the colors of rainbow- red, orange, yellow, green, blue, and violet fall within the visible spectrum. The optical transmission uses wavelength which is above the visible light spectrum and thus is undetectable to the eyes.

The typical transmission wavelengths are 850 nanometers (nm), 1310 nm, and 1550 nm.

Both lasers and LED's are used to transmit light through optical fiber. Lasers are usually used for 1310 or 1550 nm. LED's are used for 850 or 1300 nm.

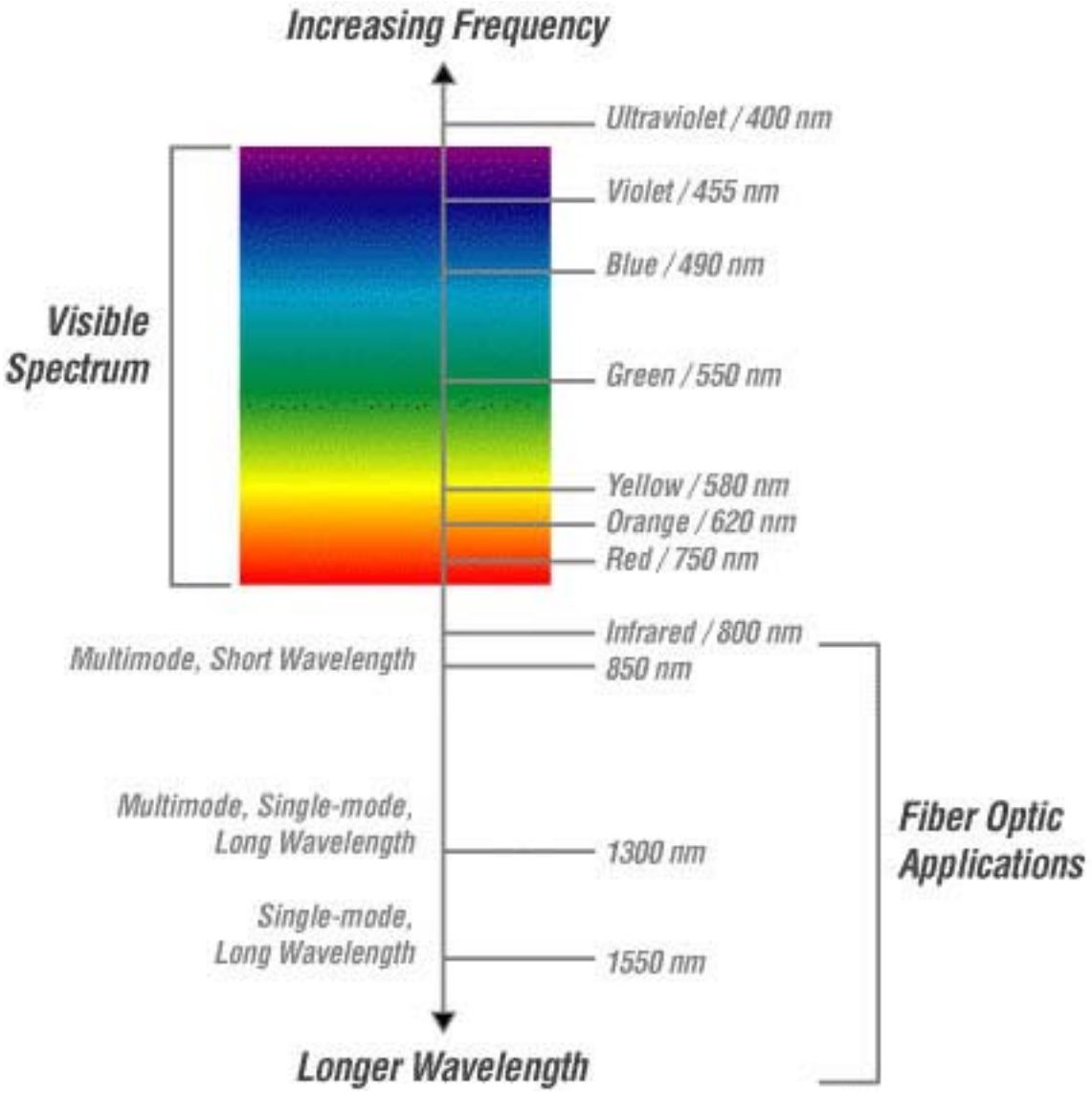



Figure 4.8 Wavelength ranges for various application

**Windows:**

The fiber operates best on particular range of wavelengths. Each range is known as operating *window.*

| Window | Operating Wavelength |
|---|---|
| 800nm - 900 nm | 850 nm |
| 1250 nm - 1350 nm | 1310 nm |
| 1500 nm - 1600 nm | 1550 nm |

**Frequencies:**

The speed of modulation of the digital or analog output of light source is called the frequency. In other words the number of pulses per second emitted from the light source is known as frequency. It is measured in hertz (Hz), where I Hertz is equal to 1 pulse or cycle per second. Figure 4.9 illustrates the frequency. Frequency is also measured in megahertz (MHz) or millions of pulses per second optical communications.

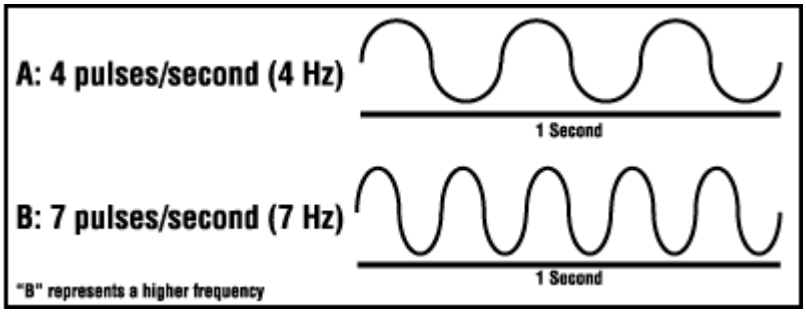



Figure 4.9: Measurement of frequency is fiber transmission

**Attenuation and Dispersion:**

Attenuation is a measure of loss of signal strength or light power that occurs as light propagates through a run of multimode or single-mode fiber. Measurements are typically defined in terms of decibels or dB/km. Over a set distance, a fiber with a lower attenuation will allow more power to reach its receiver than a fiber with higher attenuation.

Dispersion is "spreading of a light pulse as it travels down a fiber. As the pulses spread or broaden, they tend to overlap and are no longer distinguishable by receiver as 0s and 1s. Light pulses launched close together that spread too much results in error and loss of information.

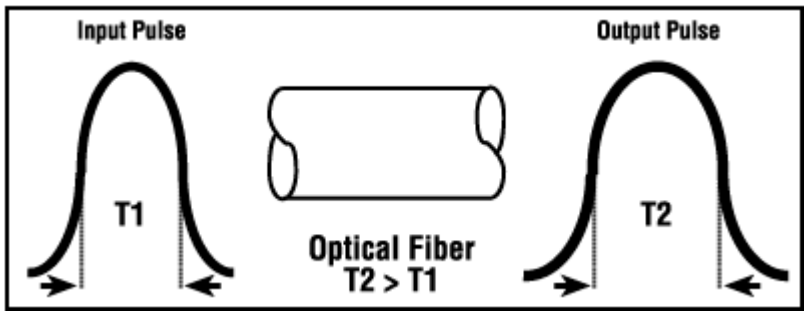



Figure 4.11: Dispersion in fiber transmission

Dispersion occurs as a result of range of wavelengths in the light source. Light from lasers and LED's consists of a range of wavelengths. Each of these wavelength, travel at slightly different speed. Over a distance, the varying wavelength speeds cause the light pulse to spread in time.

Attenuation is caused by several factors, but generally placed in one of the two categories.

- Intrinsic attenuation
- Extrinsic attenuation

*Intrinsic attenuation* is due to some impurities is the glass during manufacturing process. When a high speed signal hits the impurity in fiber, the signal shall either be scattered or be absorbed. 96% of attenuation in fibers is caused by scattering. The light travels in the core and interacts with the atoms in glass. The light waves elastically collide with the atoms and light is scattered as a result. If the scattered light maintains an angel that supports the forward travel within the core, no attenuation occurs. However if the light is scattered at an angel that does not support forward travel, the light is diverted out of the core and attenuation takes place.

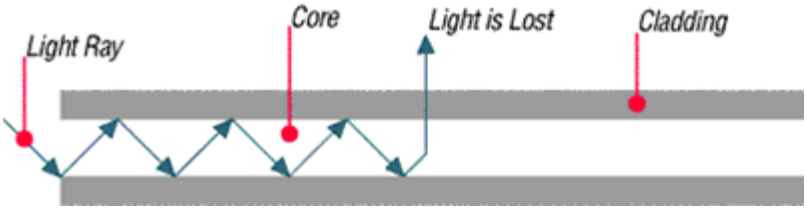



Figure 4.12: Attenuation by scattering in fiber transmission

Attenuation in fibers by way of absorption is 3.3%. This is caused due to the fact that signals are absorbed by natural impurities in the glass, and converted to vibrational energy or some other form of energy.

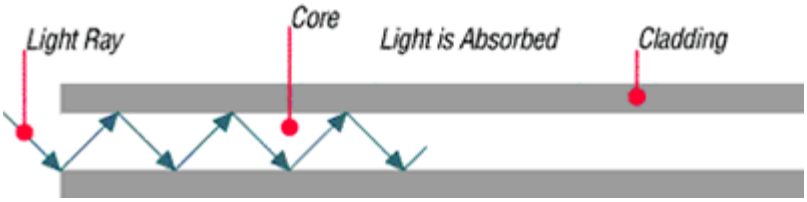



Figure 4.13: Attenuation by absorption in fiber transmission.

*Extrinsic Attenuation* can be caused by two external mechanisms:

- Macrobending
- Microbending

If a bend is imposed on an optical fiber, strain is placed on the fiber along the region that is bent. The bending strain will effect the refractive index and optical angle of the light ray in that specific area. As a result, light traveling in the core can refract out, and loss occurs.

All fibers have a minimum bend radius specifications that should not exceed.

For single mode fiber radius is 1:1/2”; 10 times the cable’s outer diameter for non-armored cable; and 15 times the cable’s outer diameter for armored cable.

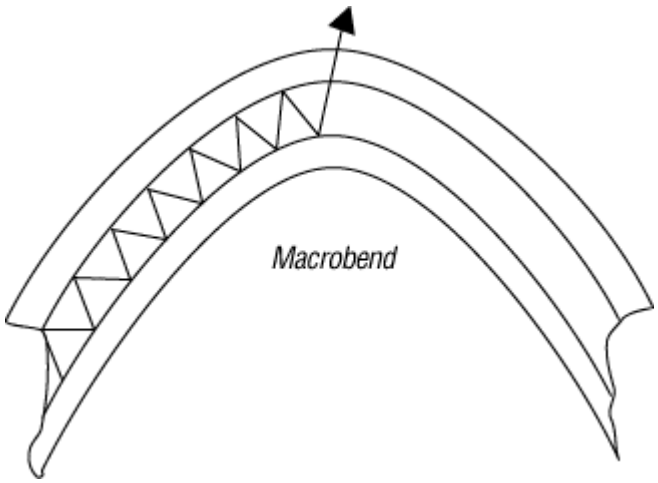



Figure 4.14: Attenuation by Macrobending in fiber transmission

Microbending is caused due to pressure on fiber. It may be related to temperature, tensile stress, or crushing force. Microbending cause a reduction of optical power in glass. (figure 4.15)

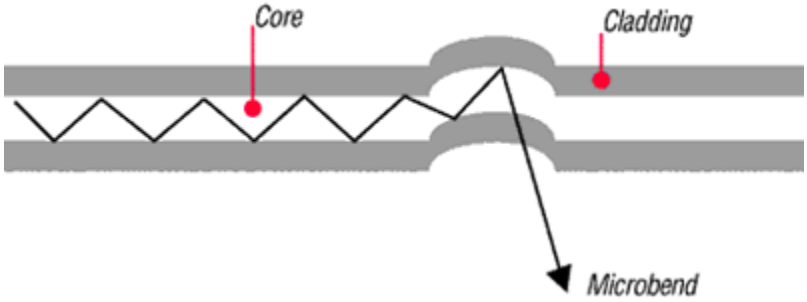



Figure 4.15: Attenuation by microbending in fiber transmission

**Bandwidth:**

Bandwidth is the amount of information a fiber can carry so that every pulse is distinguishable by receiver at the end. (Figure 4.15)

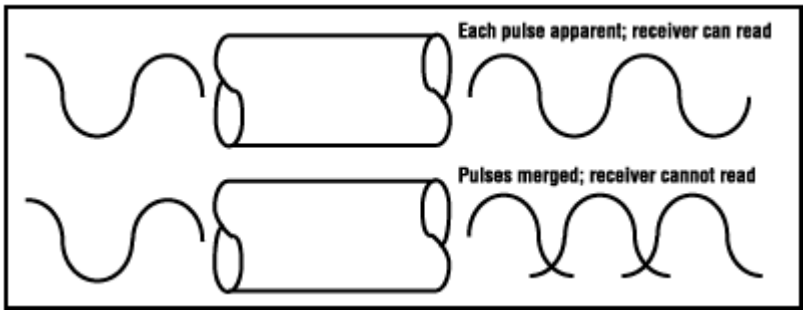



Figure 4.15: Roll of bandwidth in fiber transmission

The dispersion causes light to spread. The spreading of light pulses causes them to merge together. At a certain distance and frequency, the pulses become unreadable by receiver. The multiple pathway of multimode fibers cause this overlap to be much greater than single mode fiber. These different paths have different lengths, which cause each mode of light to arrive at a different time.

System bandwidth is measured in megahertz (MHz) at one km. In general when systems bandwidth is 200 MHz. km, it means that 200 million pulses of light per second will travel down 1 km (100 meters) of fiber, and each pulse will be distinguishable by the receiver.

## 4.3.3 ADVANTAGES OF OPTICAL FIBERS OVER COPPER - WIRES:

- Optical fibers are light in weight and occupy less space
- The attenuation of signals in optical fibers is much smaller and superior integrity found in optical systems allow much longer interval of signals transmission than metallic based systems
- Optical fibers can withstand environment hazards and have longer life than copper wires.
- In optical fibers, the electrical noise does not interfere with the propagated signal.
- Optical fibers have much greater band width than copper wires.
- Optical fibers are non inductive and non conductive so that there is no radiation and interference with other system
- The speed of transmission is very fast because the signals are carried by light.
- Data can be transferred digitally rather than analogically.

## 4.3.4 APPLICATIONS OF OPTICAL FIBERS:

The application of optical fibers has a diverse field. Some of the applications are listed below:

1. *Communication*: Optical fibers are used to carry signals in optical communication because of their unique advantages, viz. large channel capacity, wide bandwidth, good electrical isolation, no cross talks etc., Television, Telephone Satellite and Computer links of advanced communication system rely heavily on fiber optics technology.
2. *Scanning***:** Fibers are useful to measure the light intensity distribution over an illuminated area. The input end of the fiber scans the area, and the light out put is fed to the detector. The variations read by the detector output, indicates the intensity distribution.
3. *Transfer of infrared and ultraviolet energy:* Fibers are used to transfer infrared energy from the source to the point of application of heat. They are employed in ultra-violet region for spectrophotometric work.

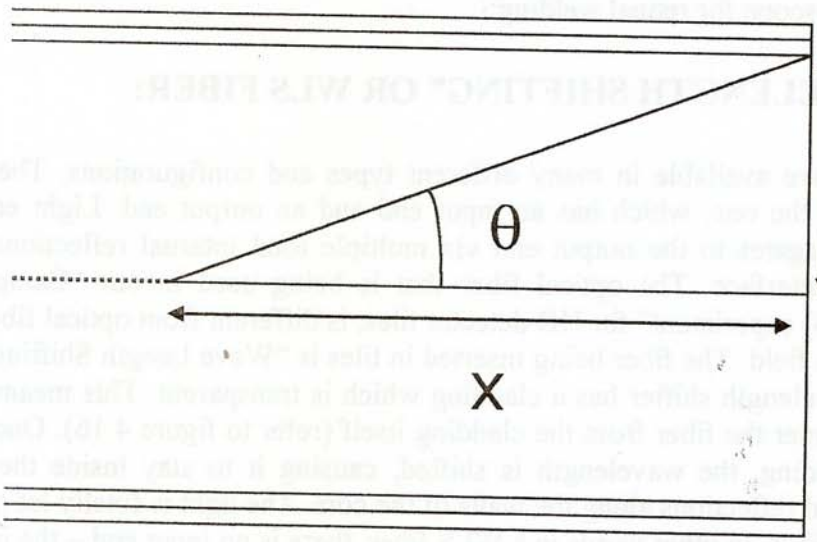
4. *Display and illumination:* For display units fibers carry light for illuminating dials when measuring units are used in dim light.
5. *Coupler:* Two circuits can be coupled to each other with the help of fibers without making any electrical link. In one circuit, the electrical signals are converted into light signals with the help of LED's and in the second the light signals are again converted into electrical signals with the help of photo detector.
6. ***Medical Use:*** Wounds are illuminated inside the human body for direct viewing. Fibers are further used in medical endoscopy, bloodless surgery, and laser othalmoscope for retinal welding.

### 4.3.3 "WAVELENGTH SHIFTING" OR WLS FIBER:

Optical fibers are available in many different types and configurations. The "normal" optical fiber is the one, which has an input end and an output end. Light entering the input end propagates to the output end via multiple total internal reflections from the core-cladding interface. The optical fiber that is being used in our "Campact Muon Solonoid (CMS) experiment" for HO detector tiles, is different from optical fibers used in communication field. The fiber being inserted in tiles is "Wave Length Shifting Fiber" or WLS. The wavelength shifter has a cladding which is transparent. This means that light radiation can enter the fiber from the cladding itself (refer to figure 4.16). Once the light enters the cladding, the wavelength is shifted, causing it to stay inside the fiber and undergo internal reflections along the walls of the core. The light is finally let out through the end of the fiber. In other words in a WLS fiber, there is no input end – the input end is the whole length of fiber. Light can enter all along the length of the fiber and not any point in particular.

Optics of the calorimeter tile consists of two components, the scintillating tiles and the wavelength shifting (WLS) fibers. Ionizing particles crossing the tiles induce the production of light in the base material with wavelength in the UV range that are subsequently converted to visible light by scintillating dopants. The scintillating light propagates through the tile to its edge where it is collected by WLS fibers. The flour in the fiber absorbs the blue light from the scintillator and re-emits it at a longer wavelength.

The fiber collects light from scintillation tiles. The light propagates along the fiber by total reflection. The light collection should be efficient, fast, with low attenuation and fibers should be radiation hard. The fibers are commercially available which fulfill the requirements are produced by Bicron, Kuraray and Pol.Hi.Tech. Out of these Kuraray fibers are chosen for the scintillation tiles in CMS experiment at CERN.




With θ = 30°, r = 1 mm;
x = 1.5 mm before photons travel along edges of fiber

Figure 4.16: “Wavelength Shifting Fiber” Schematic

## *4.4 COMPUTER CONTROLLED FIBER SCANNER MACHINE:*

For the use of WLS fiber in scintillation tiles, it is desirable to know the attenuation length of the fiber being used. Attenuation length is the length in which signal amplitude drops by some factor. A fully computer controlled scanning machine is therefore designed developed and fabricated in the Physics Department Panjab University Chandigarh. The photo in figure 4.17 shows the fabricated machine.

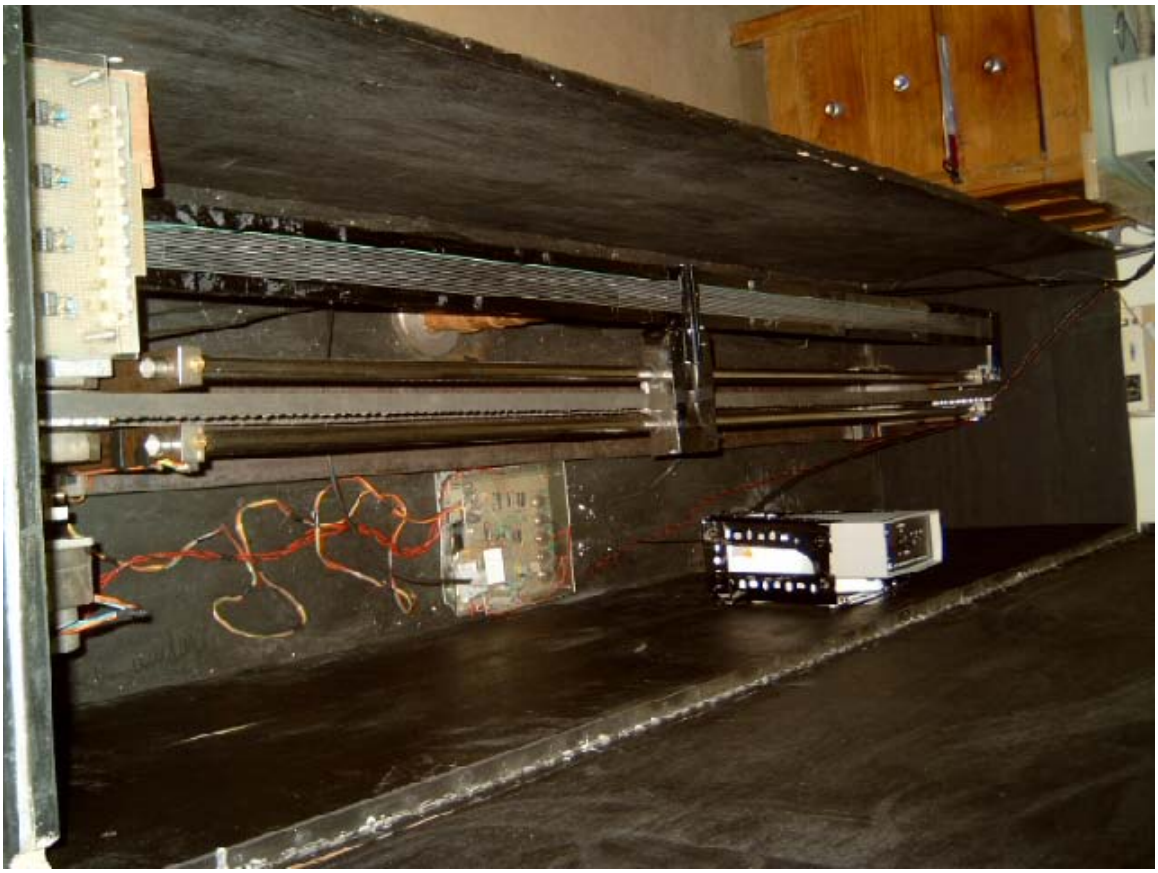


Figure 4.17: The Fabricated Fiber Scanner Machine at Panjab University Chandigarh

Thus a machine is made to check:

1. The attenuation of the wave length shifting (WLS) fiber.
2. Light transmission across the spliced region of WLS fiber and clear fiber.

Basically UV light source is to be used as input source for the fiber under test. The UV light source has to provide constant light at various points across the length of fiber. Therefore machine to be made for testing of fiber has following mechanical jobs:

1. Holder for UV light source to be made.
2. Movement of light source across the length of fiber to be established. Stepper Motor Driven Mechanical System is to be made (SMDMS). SMDMS shall give good resolution and accuracy in the Lamp's movement.
3. Platform for mounting 16 fibers at time to be made in such a way that equal light from the light source falls on the 16 fibers at given distance.
4. The output light is to be read by the photodiodes. Therefore fiber holder to hold 16 fibers is to be designed and made so that the output light falls directly on the photodiodes for further registering in the computer.
5. The whole assembly is to be installed in a light tight black box to avoid any other light falling on fiber accept UV light source.

Since pulley driven technique already existed at TIFR Bombay, we thought of making the same in our department after some rough ideas were taken from there. The principle of this method is similar to the one that is being used in printers to move the printer head. In our case it is UV Source instead of Printer head. Two pulleys of 124 mm diameter and having 28 teeth were chosen to drive a timing belt of the width 20 mm and 14mm pitch. The teeth of the pulley match with the teeth of belt. One pulley is used as driver and the other is driven. The driver pulley is driven by a stepper Motor.

The pulleys are mounted vertically on metal brackets and fine ball – bearings are used for smooth movement. The two pulleys have belt around them and on the belt UV Source holder is clamped. Two tube rods of length 2.2 Mts. in length and 3/4" diameter are being used as guide to help the light source to slide. Two L –shaped brackets are used to hold the tubes at a height of 170 cm and the distance between the two is kept 60 mm. The source holder is made such a way that is glides on the tubes. So the UV source mounted on the source holder shall move along the length of the belt.

One metallic platform is being made, to hold 16 fibers at a time and is mounted on the machine at a height, so that the distant between the UV source and fiber is kept close. A special mechanical arrangement is made to hold the motor which is mounted with gears of ratio 1:4 which drives the pulley. Nylon gears are being used, which help in absorbing the vibrations due to stepper motor. These gears do not require any oil etc. All the above mentioned brackets are being mounted on an Iron channel and the whole assembly is installed in a light black box.

The block diagram (4.4.6) explains the basic components of the fiber scanning machine. The stepper motor dives the pulley. The movement of pulley drives the belt and the lamp moves as the belt moves. Motor wires are connected to driver and control circuit (motor driver card) and also to 12 V/5 Amp Power supply unit. UV lamp source (Pencil) procured from M/S Oriel Instruments is being mounted on the lamp holder. The lamp is further linked to the special power supply, supplied by the firm and is required to put on the pencil lamp.

A special strip is designed to hold the sixteen number of fibers at one end where the light comes out of each fiber. Each fiber is fixed on this strip in such a way that the end of the

fiber just touches the front of the photodiodes fixed on the same strip. Photodiodes are further connected to the Fiber Read Out Electronics Circuits (Fiber Read Out Card). Motor driver card and fiber read out card are further linked to I/O Interface card which is installed in Pentium, via 25 pin connector. 37 pin connector is used at interface end. The details of pin connection of 25/37 pin connectors is given in table 1 and table 2.

### 4.4.1 LIGHT SOURCE FOR FIBER SCANER: (Pencil Style Calibration lamp, Model No. 6035 Hg Ar from M/S Oriel)

The lamp produces narrow, intense lines from the excitation of various rare gases and metal vapors. The 6035 Hg(Ar) lamp is insensitive to temperature and its average intensity is constant and reproducible and has long life. The lamp is called pencil type because of its shape. Lamp is shown in figure 4.18 with the dimensional diagram along with. It is made of double bore quartz tubing with two electrodes at one end sealed into a phenolic handle. A 1 ft long cord with connector is attached with the end of the handle for connection to the power supply.

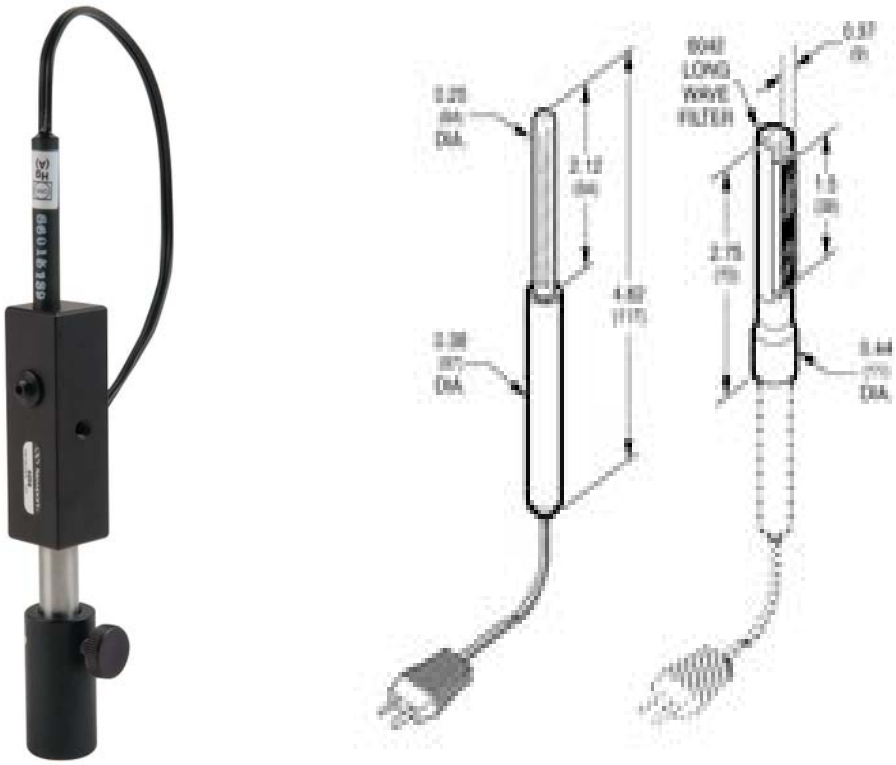


Figure 4.18: Pencil Style UV Lamp Model 3035 from Oriel

## 4.4.2 POWER SUPPLY FOR THE UV LAMP:

A special power supply model 6061from Oriel is being used for the lamp. This Supply provides, at its output, a high voltage (1200-1500V) to "breakdown" calibration Lamp and then low current to sustain the discharge through the lamp. A knob is being provided to adjust the current from 0 to 20mA for the lamp. There is polarity switch for selecting AC or DC operation and its polarity. Terminal is provided to monitor the lamp current with a DC voltmeter. 10mV=1mA lamp current.

***Operation****:* To start the lamp we first put the mode to AC. When in this mode, the current is reversed every ~30ms. Unlike normal AC power supplies, the current reversal; is not at line frequency with resulting deep modulation of the light at twice the line frequency. Instead of sinusoidal current pulses, "top hat" pulses are used with minimal reversal time.
We leave the lamp on Ac mode for few minutes till it has warmed up. We then switch to DC mode. The current through the lamp is then true DC and the light output, has very little ripples. With DC mode we can be sure of getting the same light energy in the same interval.
The current knob should not be operated once the lamp stabilized its glow. Any change during this may start creating problem and reduce the life of the bulb. If the current is reduced too much the lamp will start getting pulsated. One should avoid this operation, it may damage the bulb or the power supply.
While restarting the bulb it is important that the switch is kept on AC mode.

## 4.4.3 PHOTODIODE (S1338-5BK from Hamamatsu Japan):

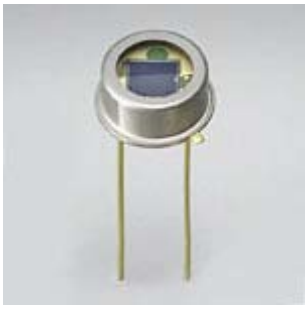
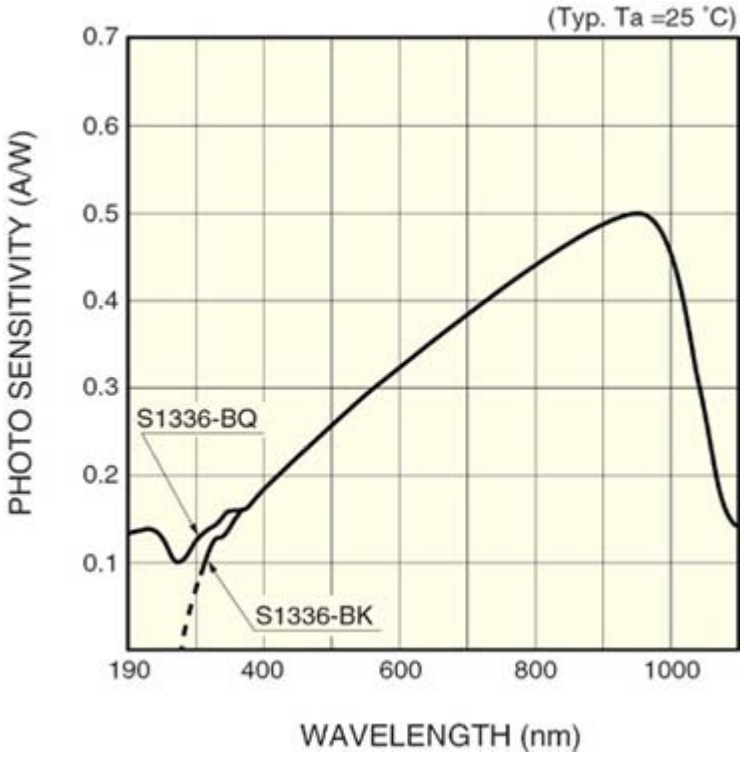
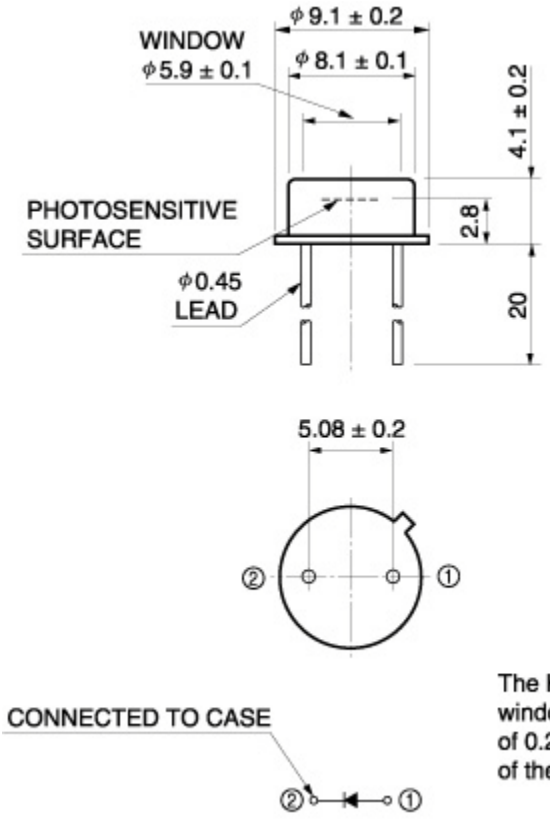


Photo diodes are light sensors that generates a current or voltage when the P-N junction in semiconductor is illuminated by light. In our fiber scanner machine we are testing our fibers for attenuation and using UV light source. The light falling on the fiber is given out at one end of the fiber which need to be read by some device. We use the photo diode for sensing the light at the end of the fiber by coupling the fiber to the photo diode. Basically the front the diode's packing has a glass window so that the light may be let fall on the Si chip for sensing and converting into current or voltage by the junction. The photodiode is further connected to an operational amplifier for further processing and amplification etc. ( See Chapter 5 for more on Photo Diodes)

***Specifications of S 1336-5BK Photo Diode:***

| | |
|---|---|
| Package | Metal |
| Package Feature | TO-5 |
| Active Area | 2.4 X 2.4 mm |
| Spectral Response Range | 320 to 1100nm |
| Photo Sensitivity at peak | 0.5 A/W |
| Dark Current Max | 0.03 nA |
| Rise time | 0.2 $\mu$s |
| Terminal capacitance | 65 pf |
| Shunt Resistance | 1 G ohm |






The K type borosilicate glass window may extend a maximum of 0.2 mm above the upper surface of the cap.

## 4.4.4 STEPPER MOTOR DRIVER AND CIRCUIT:

This circuit is designed using standard motor driver IC SAA 1027 to drive the motor in this system. It is 4-stage counter and code converter IC. Power Transistors 3055 are used to boost the power so that a stepping motor with 20 Kg.-cm torque can be driven with it. To avoid loading directly on the driver IC 1027, extra circuitry is added to provide sufficient driving current to the motor coils. The circuit is shown in figure 4.19. The clock frequency, the direction and reset pulses are being taken from PC via
Interface Card described in section 4.4.6. However for the testing of Fiber Scanning Machine, we designed a oscillation circuit by using 555 IC which could give us a square wave clock frequency of 50/60 Hz. The direction and reset pulse we gave through switches during testing. With the help of this circuit we could check the movements of the motor and thus of the lamp source and could carry out modifications in the workshop itself.

## 4.4.5 FIBER READOUT ELECTRONICS CIRCUIT:

Figure 4.20 to 4.25 explains the various circuits used in the Fiber Readout Electronics. Light from 16 Fibers is collected by 16 Photodiodes (S1336 – 5BK from Hamamantsu Photonics KK Japan) and a proportional voltage is generated by Photodiode amplifiers. Figure 4.20 shows the circuit connections of operational amplifier and photodiode.

The analog multiplexer IC MX 1616 figure 4.22 then multiplexes the outputs and feeds the analog signal to the Inverter Circuit shown is figure 4.23. The Inverted signal is then fed to the Inverting amplifier circuit shown in figure 4.24.

## 4.4.6 PC INTERFACE:

IBM – PC interface circuit controls the stepper motor and photodiode readout circuit in the fiber scanning machine. The circuit being designed by TIFR, Bombay has been duplicated and made operational by making data connecting cables (details shown in table 1 and table 2) and a software being developed to meet our requirements. The circuit used for the Interface is shown in figure 4.25. Detail of 37- D – type connectors are available in table 1 and 2.

## 4.4.7 THEORY AND WORKING OF FIBER SCANNER MACHINE:

In CMS experiment, WLS fibers are used to collect light in scintillator tiles in the detector technology. Using the WLS fibers, one can concentrate the light from the scintillator to the smaller cross section of fibers and a smaller photocathode area. WLS fibers were therefore to be tested for light output with one end fixed near a photodiode and other being treated with various reflecting materials. The fibers were being tested with far end being sputtered with Al, and checked for light output. With the help of the fabricated machine, these fibers could be tested before use for the tiles in HO detector part. (The plastic in these fibers has been doped with special dyes that absorb the blue

light from scintillator and re-emitt green light. The light is transmitted through the fiber to a hybrid photo diode (HPD). Light produced by an ionizing particle inside the scintillator is observed by the WLS fiber and re-emitted green light is guided by total internal reflection to HPD. For the transportation of light to HPD the WLS fiber is coupled to the clear fiber. The clear fiber allows the transportation of light to HPD without significant attenuation.

We are able to test ten fibers at a time as the machine is designed with ten independent channels and ten photo diodes in the fiber readout card. So ten fibers are placed on the grooved platform provided in the machine. Non Sputtered end is hooked up to each photodiode and light is allowed to fall directly on it. The output is registered on the computer as function of output signal voltage and the distance of the light source from the fiber. The light is being let fall on the fiber at variable lengths from the end of the fiber (which is coupled to the photodiode) with the help of the stepper motor which makes the movement of the light source across the length of ten fibers placed on the platform. The movement of the motor for varying the distance is maintained by the computer controls.
The intensity pattern is represented by sum of two exponentials of the form

$$I(x) = A1 \times e^{-x/\alpha_1} + A2 \times e^{-x/\alpha_2}$$

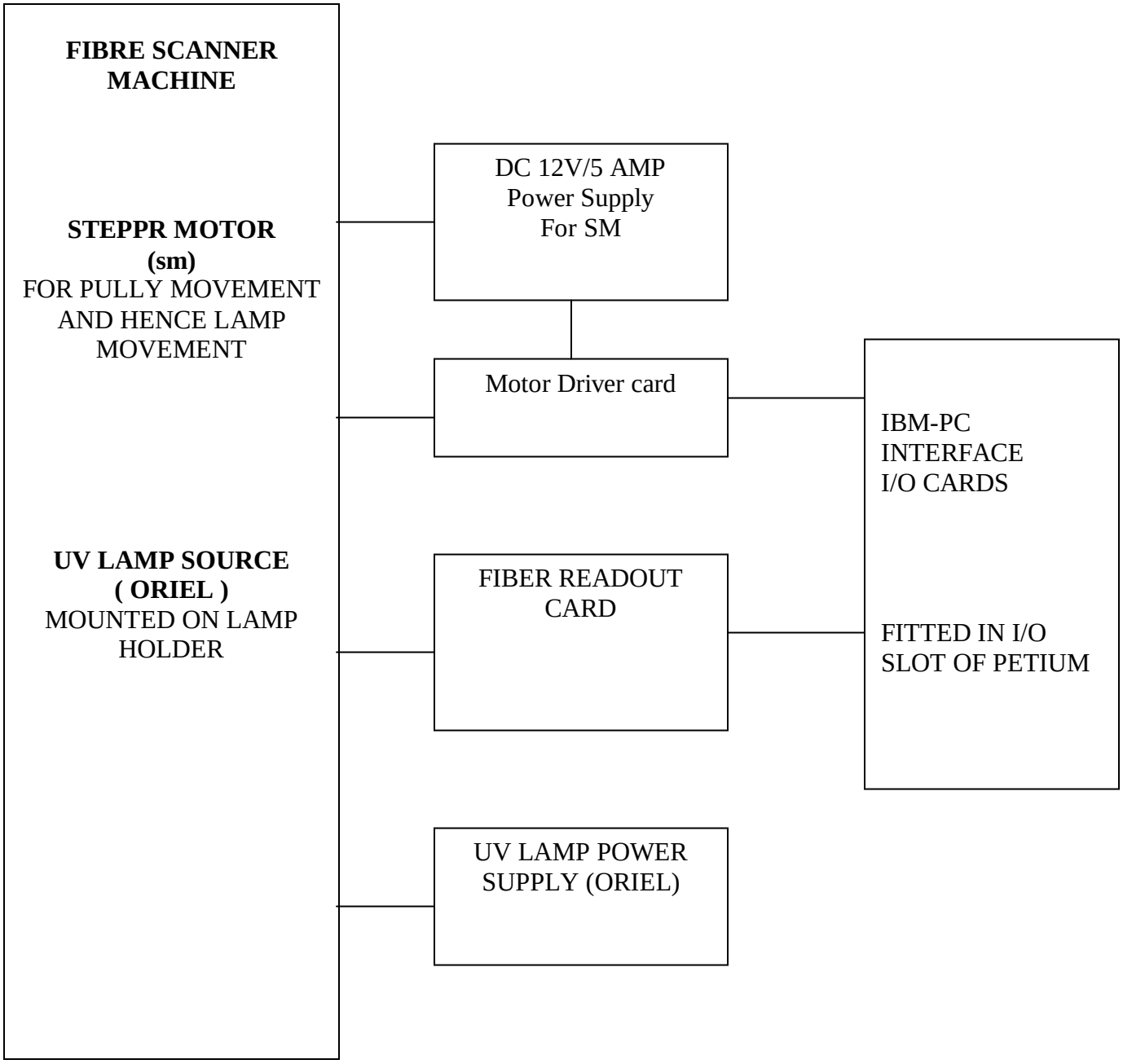
Where A1, A2, $\alpha_1$, $\alpha_2$ are fitted parameters [13]

Number of fibers are being testing on the scanner machine and one such example of the tested fiber is given in table and is depicted in figure 4.26. It is shows that the intensity pattern is represented by sum of two exponentials as given by the equation above.

***Precautions:***

1. The distance between the fiber and the UV source should be close and constant across the length of the fiber. The alignments may be done from time to time and corrected if needed with the help of the screw adjustment lever below the fiber platform.
2. Only Nylon gears are the best for absorbing the vibrations due to Stepper Motor. In case of replacement same type of nylon gears should be used.
3. The whole assembly need to be kept in a light tight black box to avoid light interferences from outside.
4. The grooves on the fiber platform should be clean and dust free or otherwise you may not be able to maintain the distance between the light source and the fiber.
5. Lamp operation should be followed strictly as per the guidelines by the manufacturer i.e. the lamp should be operated on AC mode first and then switched over to DC mode after it has glowed to its proper intensity.
6. For every set of readings the machine should be initialized first and brought to the start point.

## 4.4.8 BLOCK DIAGRAME OF FIBER SCANER MACHINE:



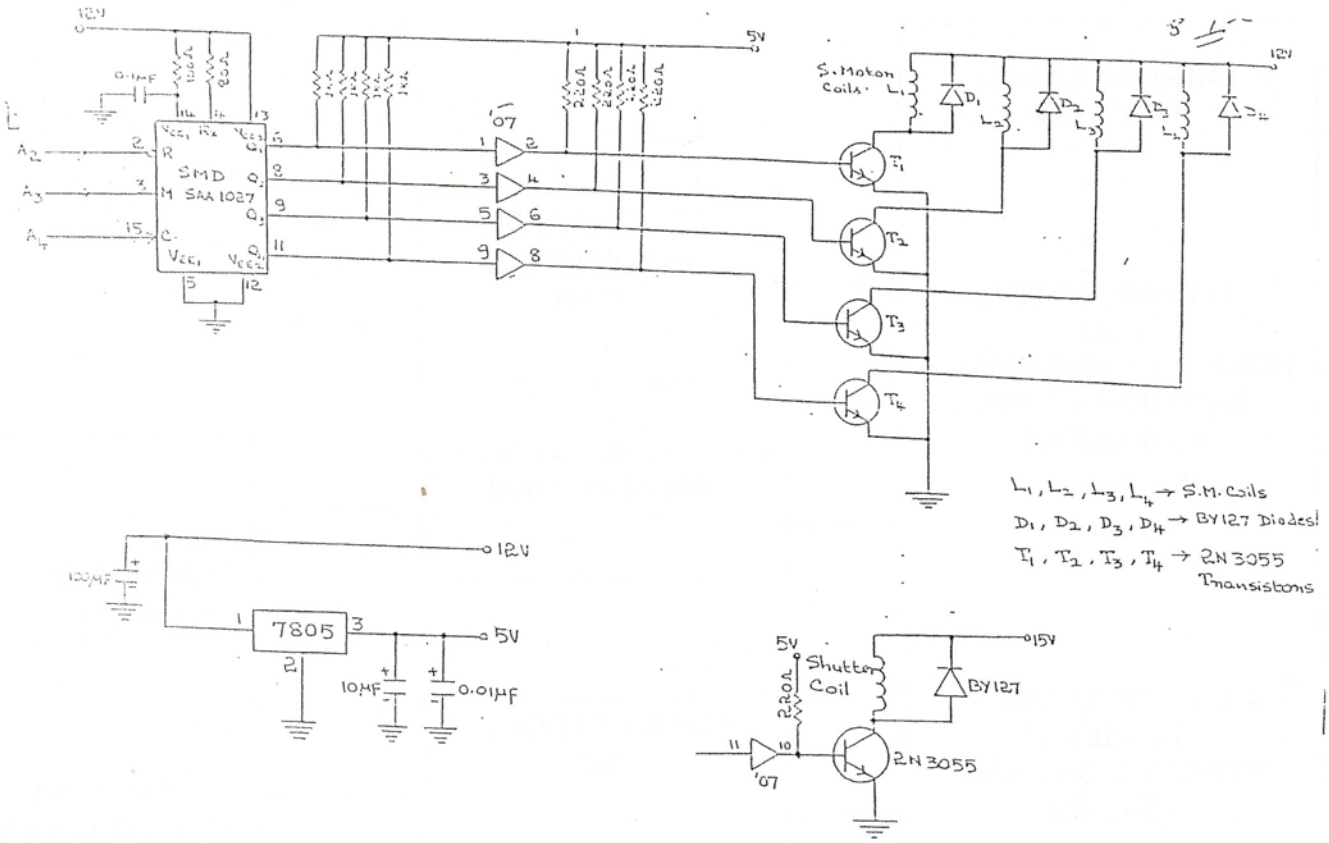



Figure 4.19 Stepper Motor Driver And Control Circuit

# PHOTO DIODE READOUT FOR FIBER SCANNER

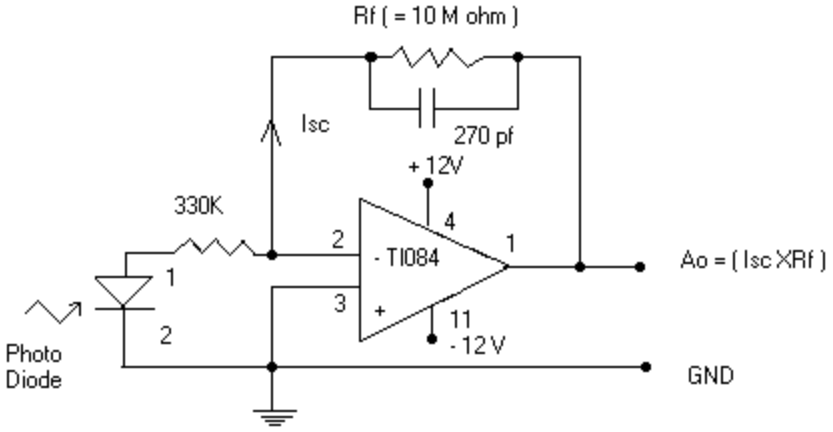



Figure 4.20: Pick-up Circuit ( one per channel)

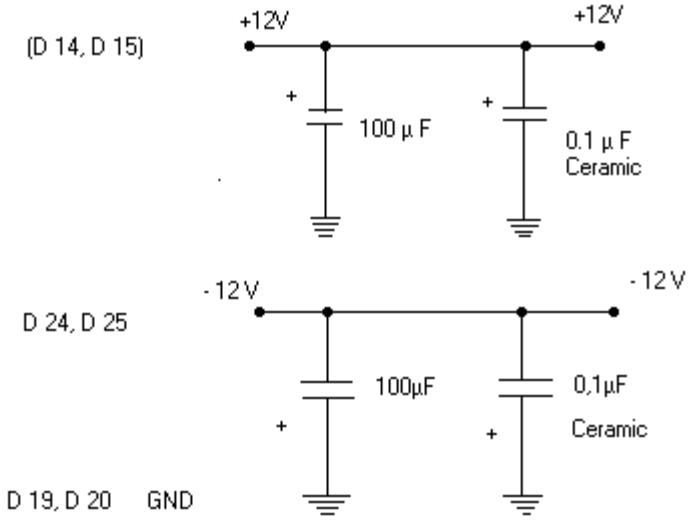



Figure 4.21: Supply Circuit for TL 084 IC

# PHOTO DIODE READOUT FOR FIBER SCANNER

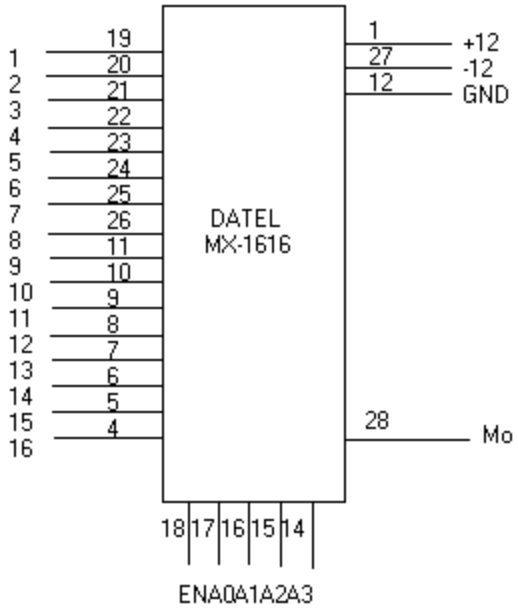



Figure 4.22: Analog Multiplexer

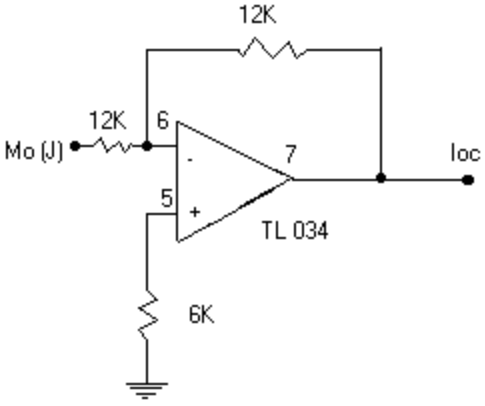



Figure 4.23: Inverter

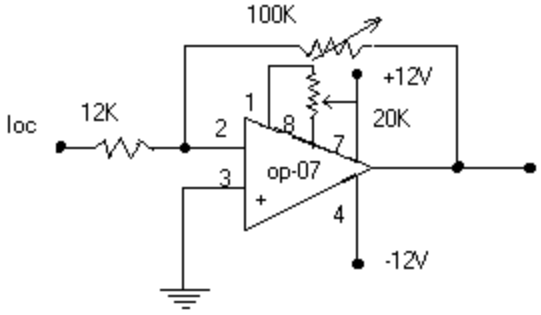



Figure 4.24: Inverting Amplifier

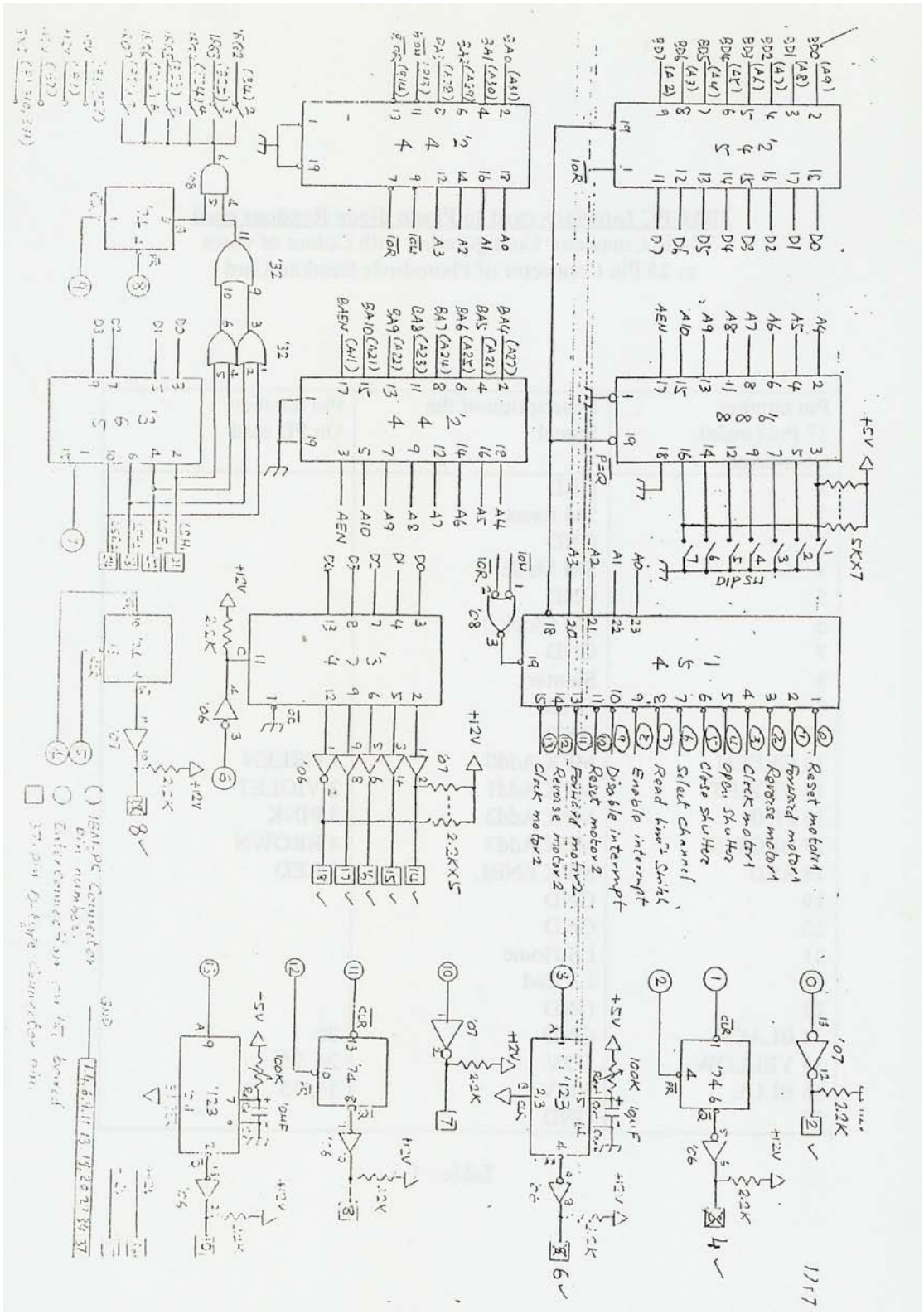


Figure 4.25 IBM PC INTERFACE FOR DUAL STEPPER MOTOR & PHOTODIODE READOUT- CONTROLL

**IBM-PC Interface card to Photo diode Readout card**

37-Pin Connector Configuration with Colour of wires
to 25 Pin Connector of Photodiode Readout Card

| Pin number<br>37 Pin (male)<br>Connector | Description of the<br>Signal | Pin number<br>On PD card |
|---|---|---|
| 1 | GND | |
| 2 | SM Reset | |
| 3 | GND | |
| 4 | SM Mode | |
| 5 | GND | |
| 6 | SM Clock | |
| 7 | GND | |
| 8 | Shutter | |
| 9 | GND | |
| 13 | GND | |
| 14 GREEN | MPX Add0 | 1 GREEN |
| 15 VIOLET | MPX Add1 | 2 VIOLET |
| 16 PINK | MPX Add2 | 3 PINK |
| 17 BROWN | MPX Add3 | 4 BROWN |
| 18 RED | MPX ENBL | 5 RED |
| 19 | GND | |
| 20 | GND | |
| 21 | LS Home | |
| 22 | LS End | |
| 23 | GND | |
| 34 BLACK | GND | 20 |
| 35 YELLOW | -12V | 24, 25 |
| 36 BLUE | +12V | 14, 15 |
| 37 | GND | |

Table - 1

**IBM-PC Interface Card to Stepper Motor Driver Card**

37-Pin Connector Configuration with Color of wires
to 25 Pin Connector of SM Motor

| Pin number<br>37 Pin (male)<br>Connector | Description of the<br>Signal | Pin number<br>25 Pin (male) Connector<br>(SM Side) |
|---|---|---|
| 1 BLACK | GND | 1 |
| 2 GREEN | SM Reset | 2 |
| 3 | GND | |
| 4 PINK | SM MODE | 3 |
| 5 | GND | |
| 6 YELLOW | SM Clock | 4 |
| 7 BLUE | GND | 5 |
| 8 RED | Shutter | 9 |
| 9 | GND | |
| 13 | GND | |
| 14 | MPX Add0 | |
| 15 | MPX Add2 | |
| 16 | MPX Add2 | |
| 17 | MPX Add3 | |
| 18 | MPX ENBL | |
| 19 | GND | |
| 20 | GND | |
| 21 BROWN | LS Home | 21 |
| 22 VIOLET | LS End | 22 |
| 23 | GND | |
| 34 | GND | |
| 35 | -12V | |
| 36 | +12V | |
| 37 | GND | |

Table – 2

| Position (mm) | 100 | 175 | 250 | 325 | 400 | 475 | 550 | 625 | 700 | 775 | 850 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Voltage (V) | 1.77 | 1.44 | 1.25 | 1.20 | 1.14 | 1.07 | 1.03 | 1.01 | 0.93 | 0.93 | 0.90 |

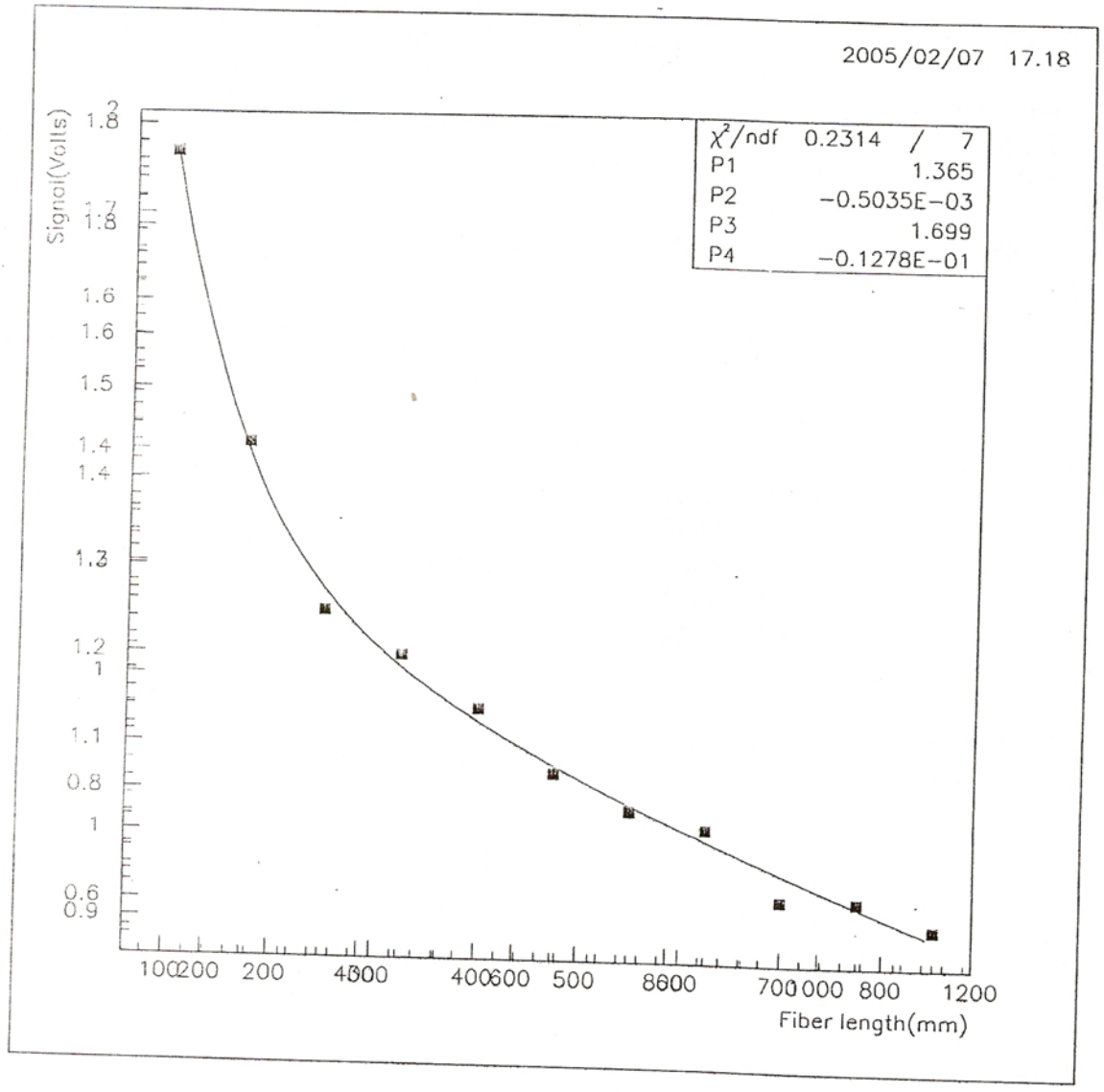



Figure 4.26: The result of a fiber tested on Fiber Scanner Machine

## 4.5 HO MODULES OF CMS DETECTOR [14]:

HO layers are geographically located inside the barrel muon system in overall CMS setup. The scintillator layers of HO are mapped to 5 rings of moun station from where the optical fibers are taken out through the space between the rings to photo detectors placed at the outer end of the ring. Muon rings are -2, -1, 0, +1, +2. There is a single layer of HO for rings -2, -1, +2, +1 where as two layers of HO for ring 0. (layer 0 and layer 1) The rings are 2.51 m long and are symmetrically positioned with respect to centre at a radius of 7.43 m. Each ring has 12 identical sectors and each sector has 6 slices. The slices of layers are identical in all sectors. Each slice is further divided into scintillator units. This single unit is called **tile**. The tile is the smallest unit of HO which is integral part of the layer in each ring of the detector.

HO has 95 different tile dimensions, 75 for layer 1 and 20 for layer 0 and a total number of tiles is 2736 (2160 for layer 1 and 576 for layer 0).

All tiles of same slice of a ring of the same layer is packed into a single mechanical unit called **tray**. The tray covers the entire length of the moun ring. Figure 4.27 shows the layout of the tile in a tray.

Each tray contains 6 tiles in ring +2,-2; 5 tiles in ring +1, -1 and 8 tiles in ring 0. The tray is covered with a piece of tyvek paper. It is further covered with tedler to prevent leakage and finally fixed between two plastic plates for mechanical support with the help of countersunk screws passing through holes. The top plastic sheet has channels grooved into it to rout the fiber from individual tiles to an optical connector located at the edge of the tray. (See figure 4.28) The top plastic cover has position for the optical connector grooved on it. There is a 1.5 mm wide groove to accommodate the ‘source Tube’ used for calibrating the modules. Each connector has two holes and they are fixed to the scintillator-plastic assembly through matching holes in them using 6 BA bolt and nut. The tile-tyvek-tedler-plastic assembly is placed in stainless steel tray covers. The tray covers have cuts for assessing the optical connectors. The complete assembled tray is shown in figure 4.29

Each sector has 6 trays. So a total number of trays is 360 for layer 1 and 72 for layer 0.

### 4.5.1 TRANSPORTATION OF LIGHT TO PHOTO-DETECTOR:

The light is collected by WLS fibers inserted inside the grooves of the tile. The collected light is transported to the photo detectors located outside the muon rings by clear fibers. The captive end of the WLS fibers located inside the grooves are polished, aluminized and is protected with a thin polymer coating. The other end of the WLS fiber comes out of the tile through a slot (3 mm X 25 mm) made on the 2 mm thick black plastic cover sheet. This end of WLS fiber is spliced to clear non-S type multi clad Kuraray fiber. The clear fiber is then routed through 1.6 mm deep guiding grooves made on outer side of the 2 mm plastic sheet to an optical connector located at the edge of the tray. Each tray has two optical connectors mounted on one side of the tray. In tray the grooves of the tiles form two rows (figure 4.27). The fibers from one row are terminated on one connector. The number of fibers from tray in different rings is given in Table in figure 4.30.

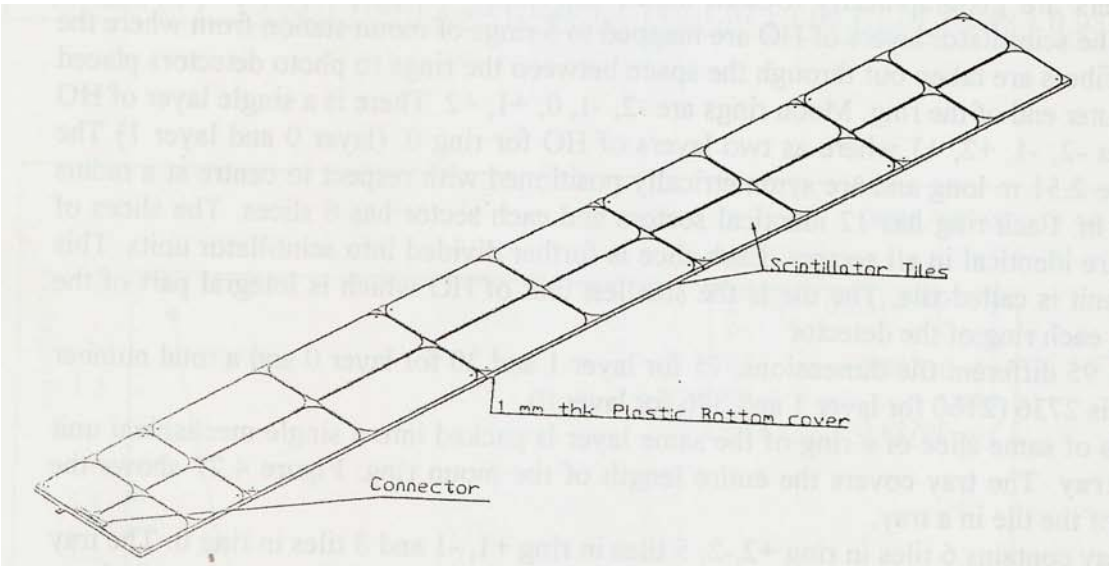



Figure 4.27: Layout of the Tiles in Tray

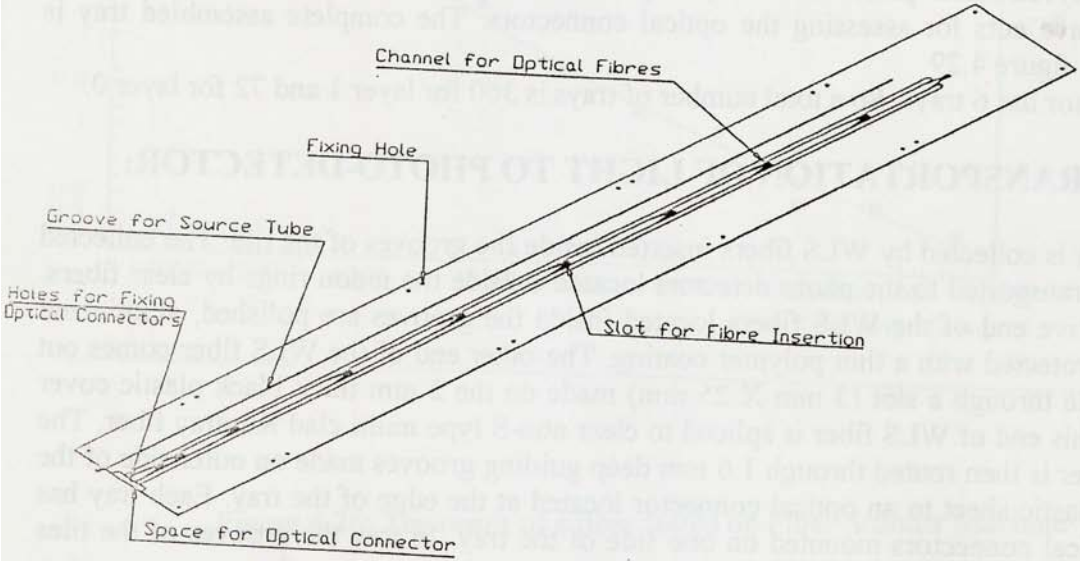



Figure 4.29: The assembled Tray consisting of tiles, plastic covers and stainless steel covers. The components are slightly displaced from their actual position to show their matching designs.

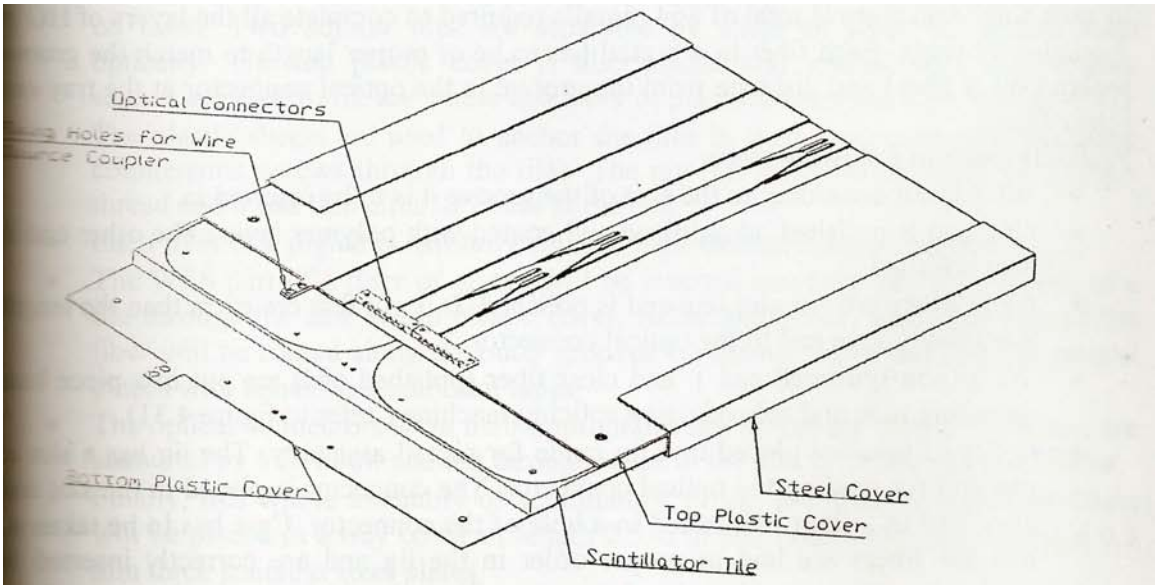



Figure 4.29: The assembled Tray consisting of tiles, plastic covers and stainless steel covers. The components are slightly displaced from their actual position to show their matching designs.

Table

| Ring | Tiles/tray | Fibers/tray | Fibers/connector |
|---|---|---|---|
| 0 | 8 | 32 | 16 |
| -1, +1 | 6 | 24 | 12 |
| -2, +2 | 5 | 20 | 10 |

Figure 3.30: Tray specifications for different rings of HO

## 4.5.2 PIGTAIL:

A bunch of fibers fixed to an optical connector is called a pigtail. There are two pigtails in each tray. And there is total of 864 pigtails required to complete all the layers of HO in 5 number of rings. Each fiber in a pigtail has to be of proper length to match the groove length (WLS fiber) and distance from the groove to the optical connector at the tray end (clear fiber).
Pigtail is made in following steps:

- WLS is cut according to the size of the groove it is to be inserted in.
- One end is polished, aluminized and coated with polymer layer. The other end is also polished.
- Clear fibers are cut and one end is polished. It is cut few cm extra than the length from the groove end to the optical connector.
- WLS (non-sputtered end ) and clear fiber (polished end) are put in a piece heat shrinking tube and spliced using splicing machine ( refer to figure 4.31).
- Spliced fibers are placed in a jig made for pigtail assembly. The jig has a slot at one end for holding the optical connector. The connector is placed in the slot and clear end of a fiber is inserted in a hole of the connector. Care has to be taken so that the fibers are laid in proper order in the jig and are correctly inserted in connector. The extra length of the clear fiber should be projecting out of the connector.
- Optical cement is prepared and poured through the socket in connector.
- The whole assembly is kept undisturbed and cured for 12 hours.
- The pigtail is removed from the assembly jig and connector is fixed in a polishing jig. First it given a rough polish, then polished with a high speed diamond cutter.

## 4.5.3 OPTICAL CABLES:

These are cables needed for transporting the light collected by pigtails in the tray to the photo detectors (Hybrid Photo Diode, HPD) located out side the moun station. The cables are connected to the fibers in trays through optical connectors. The cables will have 10, 12 or 16 fibers depending on the HO ring.

## 4.5.4 PLASTIC COVER:

Both the plastic covers are made on CNC milling machine. First plastic sheets are cut into size slightly bigger than actual size and then machined. After machining of the edges of the covers the top cover is machined for grooving.

## 4.5.5 TRAY ASSEMBLY:

Tray is fabricated in following steps:

- The tiles are cleaned and sides are painted with Bicron reflecting paint for better light collection.

- Plastic covers are also cleaned.
- Tyvek and tedler are cut according to the size of the tray holes punched in it. The holes should match with the top and bottom cover for the fixing screws and also for fibers.
- The bottom plastic, tedler and tyvek are placed properly and the tiles are placed on them. Two adjoint tiles are separated by strips of tedler to isolate them optically. The top plastic cover is also placed and special 6BA countersunk screws are used to fix the whole assembly of plastic covers and tiles. (figure 4.32)
- The plastic sheets are used to anchor the tiles in their respective position using countersunk screws through the tiles. The nut has a cylindrical shaft with 6 BA thread and it has thin circular collar at the end.
- Each fiber of a pigtail is carefully cleaned with alcohol before insertion.
- The WLS part of a fiber of pigtail will be inserted carefully into the grooves of a tile through the slot in top plastic cover, tedler and tyvek. The clear part of the fiber will be routed along the outer grooved on the top cover and fixed at several places with adhesive aluminium tapes.
- The optical connectors sit in their appropriate slot on the top plastic cover and are anchored by 6 BA bolt and nut through holes in the plastic sheets and scintillator.
- Finally, this whole assembly of scintillators, tyvek, tedler and plastic and fibers will be placed in a tray cover of length 2.536 m and height 13.8 mm made of 0.3 mm thick stainless steel plates.

## 4.5.6 MATERIALS USED FOR HO MODULES:

| Materials | Source | Specification | Dimensions (mm) |
|---|---|---|---|
| Scintillator | Bicron | BC 408 | $10^{+0}_{-1}$ |
| WLS fiber | Kurary | Multi clad, Y11 | 0.94 |
| Clear fiber | Kurary | Multi clad | 0.94 |
| Stainless steel | | | 0.3 |
| Top plastic cover | | | 2 |
| Bottom plastic cover | | | 1 |
| Tedler | | | 0.1 |
| Tyvek | | | 0.15 |
| Polyster tape | 3M | black | 0.15 |
| Aluminium tape | 3M | | |
| Optical; connectors | | Plastic moulded | |
| Reflecting paint | Bicron | | |
| Optical cement resin | Bicron | BC 600 | |
| Optical cement hardener | Bicron | BC 600 | |
| Heat shrink tube | | | |
| Black Sleeves | | | |
| Special screw and nut | | See text | 6 BA |

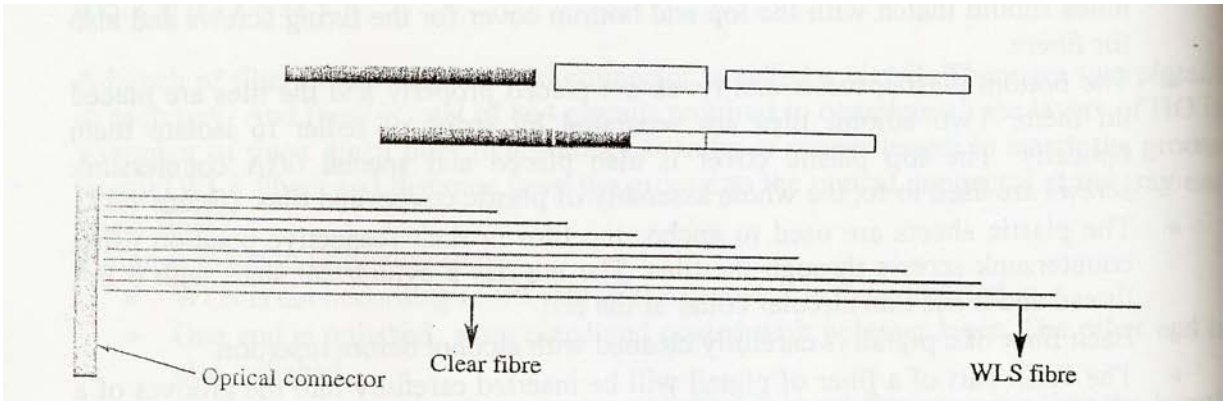



Figure 4.31: Splicing of WLS with clear fiber is shown on top figure. The bottom figure shows an assembled pigtail.

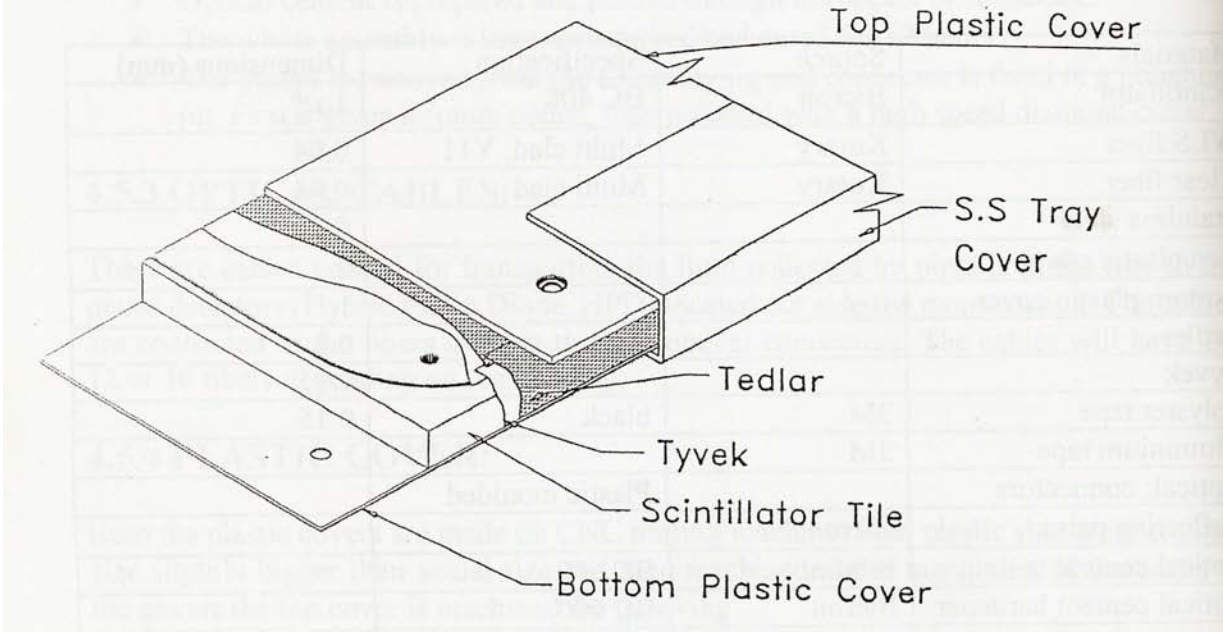



Figure 4.32: Details of the packed tray showing tiles, tyvek, tedler, plastic covers and stainless steel tray.

## 4.6 HO INSTALLATION AT CERN:

### 4.6.1 HONEYKOMB HANGING STRUCTURES:

For placing the scintillator trays in HO layer of all the 5 rings of CMS detector, a honey comb hanging structure is developed and fabricated. Each ring has 12 identical size sectors and each sector has 6 trays. Honey comb structures are therefore fabricated for each sector. Honeycomb plates are used to fabricate the hanging structures using c-channels. The size of the structure is made of the size of one sector in which 6 trays could be inserted. The figure 4.33 shows the fabricated hanging structure. Trays and hanging structures were taken to CERN separately packed. One such structure therefore, constitute one sector in a ring and 12 structures constitute the complete layer of HO. The trays are packed/inserted into the structures at CERN after testing them on X-Y scanner and analizing the results. Assembled structures with trays inserted and packed is called panel. These panels are then finally installed in each ring of CMS detector with the help of crane. (See figure 4.34). Figure 4.35 shows the HO panels in ring +2 and +1.

### 4.6.2 READOUT ELECTRONICS:

Optical signals from each tile is to be read by hybrid photodiodes (HPD) and converted into electrical signals and then passed on to data acquisition system (DAQ). Figure 4.36 shows the readout electronics box (RBX) being designed and fabricated for doing the job. Each RBX has four readout modules (RM) two on the left side and two on the right side of the picture. A calibration module (CM) is there in each RBX to calibrate the RM's. There is clock controller monitoring (CCM) just on the back of the CM. Each RBX is provided with connector on the back for high voltage (HV) cables connections and low voltage (LV) cable connections. HV and LV distribution box are plugged into these connectors to establish the connection of HV and LV to the required modules of RBX. All modules are mounted into a stable aluminium housing using slide and plug in technique, on the base of the RBX called *shell.* Figure 4.37 shows the empty shell. RM's of this shell are taken out. The back side of the shell is shown in figure 3.38. We can see the mounted copper pipes provided for cooling of each module. The copper pipe is embedded into the walls of the shell where each module is pushed in. Water is circulated in the copper pipe which provides good cooling to all the modules. Each module is fixed on the base of the shell with the help of a screw after pushing each and plugging into the corresponding connectors. The top of the RBX is covered with aluminium sheet and tightened with countersunk screws. The front and back of the RBX remains open for cabling purposes.

The read out module basically has HPD and other electronic circuitry inside it. RM and CM are provided with optical connectors for connecting the calibration cables from CM and also for connecting the optical cables from trays. Orange cables known as data cables from VME crate of DAQ are also connected to each RM (See pictures of RBX). CM is provided with a clock input cable connection from VME crate. CM has light emitting diodes (LED). The emitted light is transmitted to RM's via calibration cables to calibrate the HPD. Light of variable intensity can be thrown on each pixel of HPD and calibration

done with the help of data on DAQ. One RBX covers two sectors i.e. 12 trays. So a total of six RBX's are required for covering each ring of the CMS detector.

### 4.6.3 CABLES FOR HO

The Types of cables being fabricated and used by team for HO installation at CERN are: Optical Cables, Calibration Cables, HV Cables, LV Cables, Orange Cables for DAQ, TTC Cables, Laser Cables, DCS Cables etc.
Elaborate and involved procedures are adopted to make all these cables after calculating the path length in each ring.

### 4.6.4 BURN IN TESTING OF READOUT ELECTRONICS BOXES:

The test stand is divided into four parts:

1. *VME based data Acquisition System:*
Picture 1 of figure 3.39 shows the the VME crate used alongwith the PC for storing and analizing the QC data. DAQ is cabled to readout box (RBX) via orange cables for to and fro transfer of data. VME data bus is going to the PC for storage. HO testing program is run to store data on to the PC.

2. *PC for setting HV, LV, LED Intensity control and temperature monitoring:*
Picture 2 in figure 3.39 shows the PC used for setting up variable voltages and intensity of LED. Cables are used to linkup each module for setting and monitoring during testing of RBX.

3. *LV and HV Stand:*
Picture 3 in figure 3.39 shows the stand for both LV and HV. The stand also has LAN switch for separately linking up each module to the PC. HV, LV and intensity of LED is set using software in the PC and data taken on the other PC attached to DAQ. All hardware settings are monitored and stored in this PC. Monitoring of settings and temperature helps in knowing about the proper functioning of the RBX. Modifications and corrections are carried out in the RBX using the monitored data.

4. *BURN IN test stand:*
Picture 4 in figure 3.39 shows the stand. After testing each RBX separately at 8KV, 9KV,and 10 KV and different intensity, each RBX is put to burn in test for 7 days. Three RBX could be put in this stand for burn in with actual cables to be used for final installation in the ring. Cooling connections are established to circulate water in all the three RBX before start of burn in test via DAQ PC as well as setting and monitoring PC. Data is monitored every day and studied for any change in characteristics of modules of the RBX during burn in. Final data is taken after seven day burn in test of the group of three RBX's. Each RBX is kept ready and place in the ring assigned, after it has passed the burn in test.

Figure 4.33: The fabricated hanging structure with 6 trays inside is ready for installation as HO layer in one of the rings in CMS detector

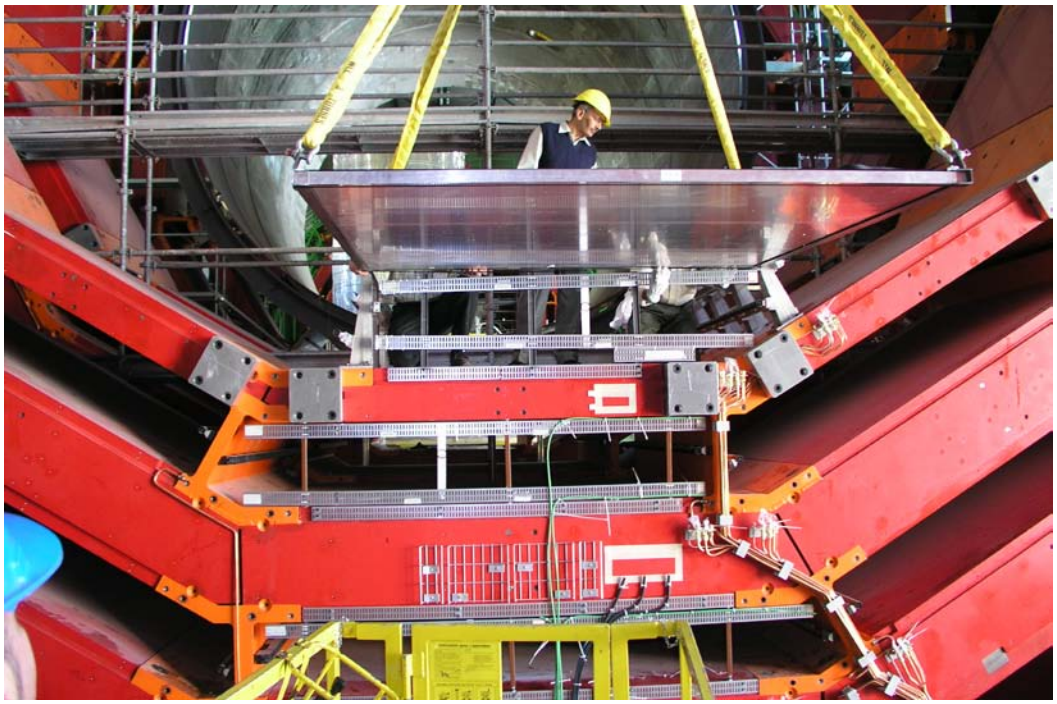


Figure 4.34: The panel being carried by a crane for final insertion in the ring

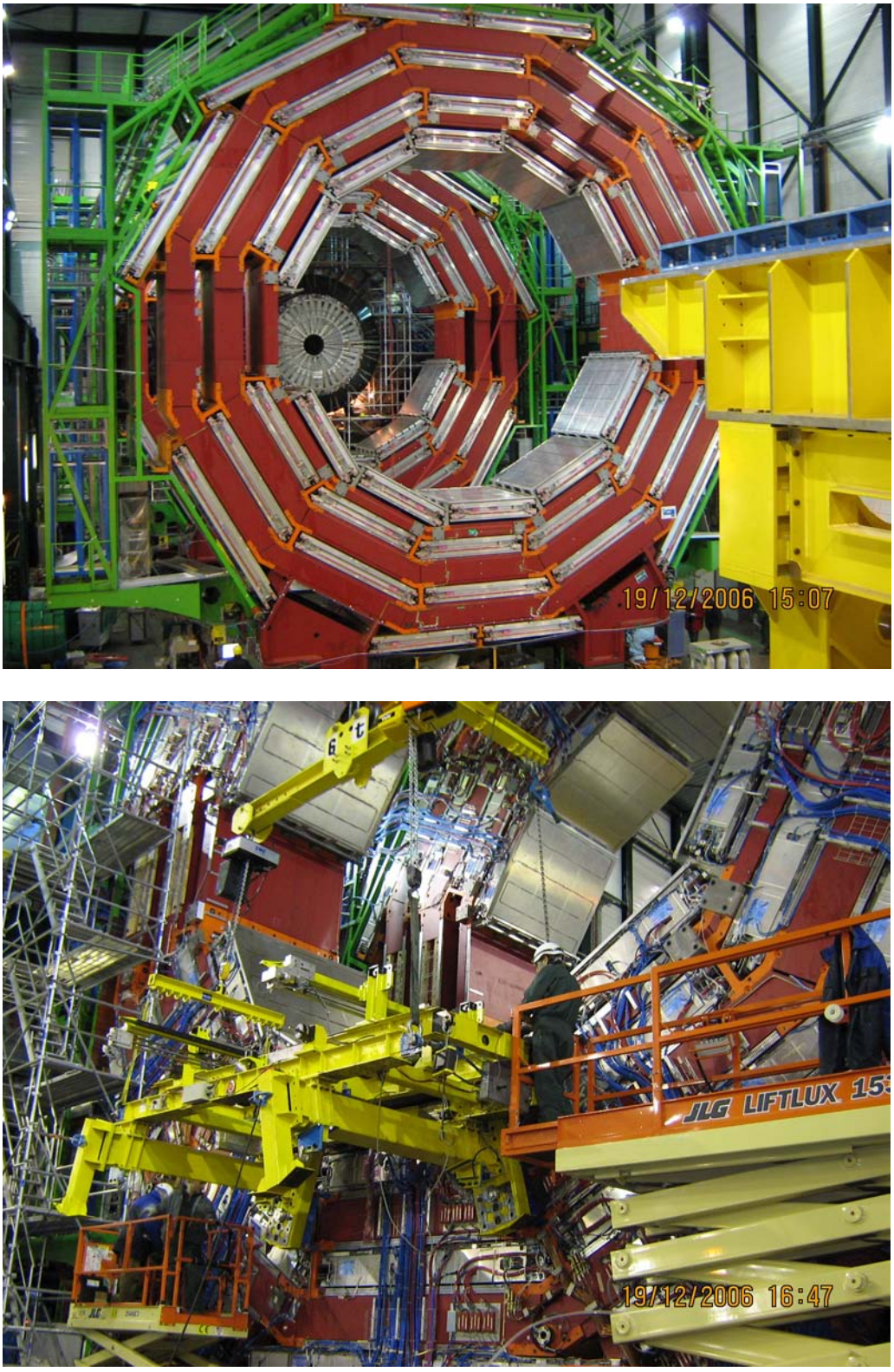



Figure 3.35: View of the HO Panels having been installed in ring +1 and +2

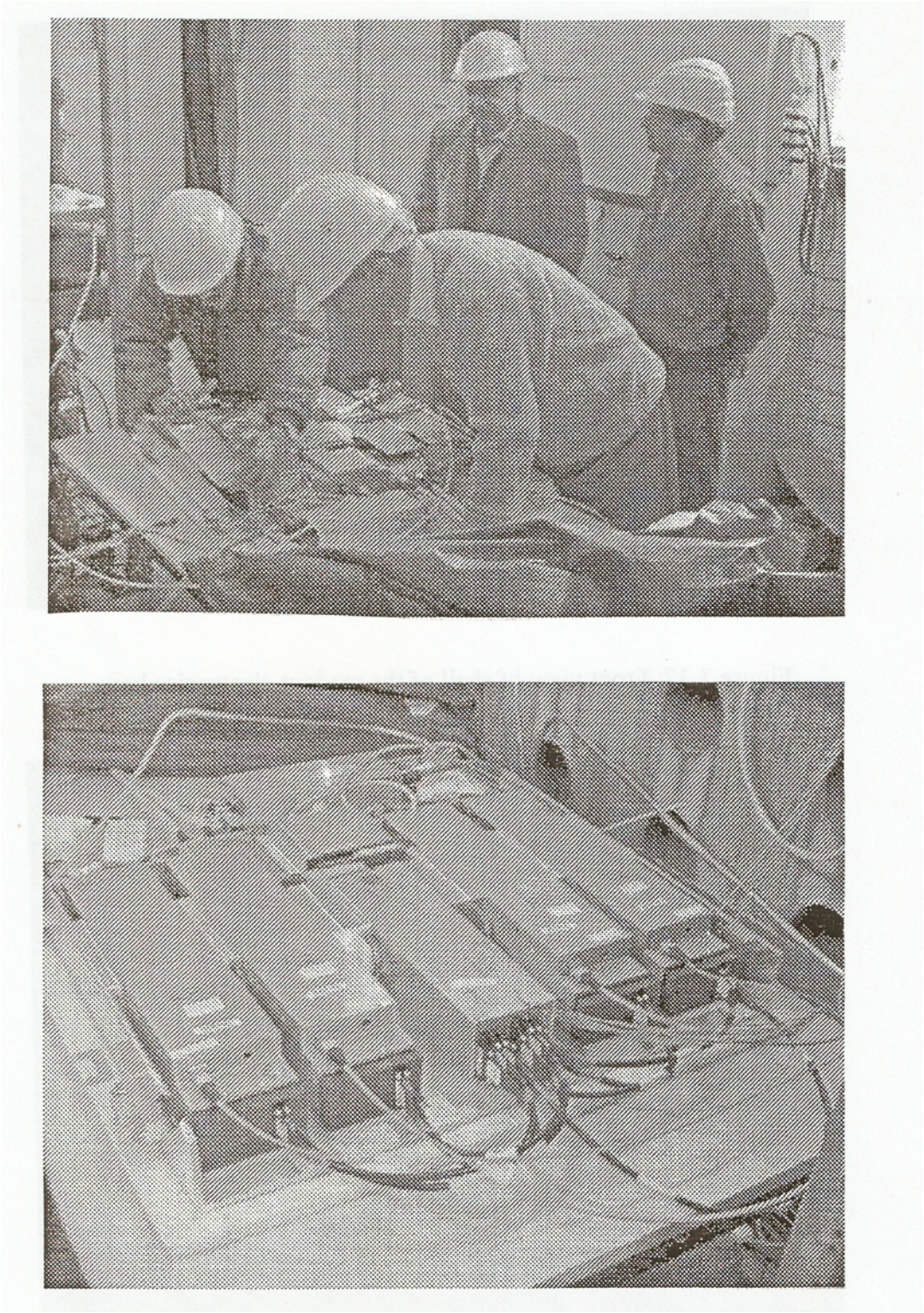


Figure 3.36: The Readout Electronics Box under test showing Calibration cables, Orange cables from VME crate, HV, LV cables and cooling connections

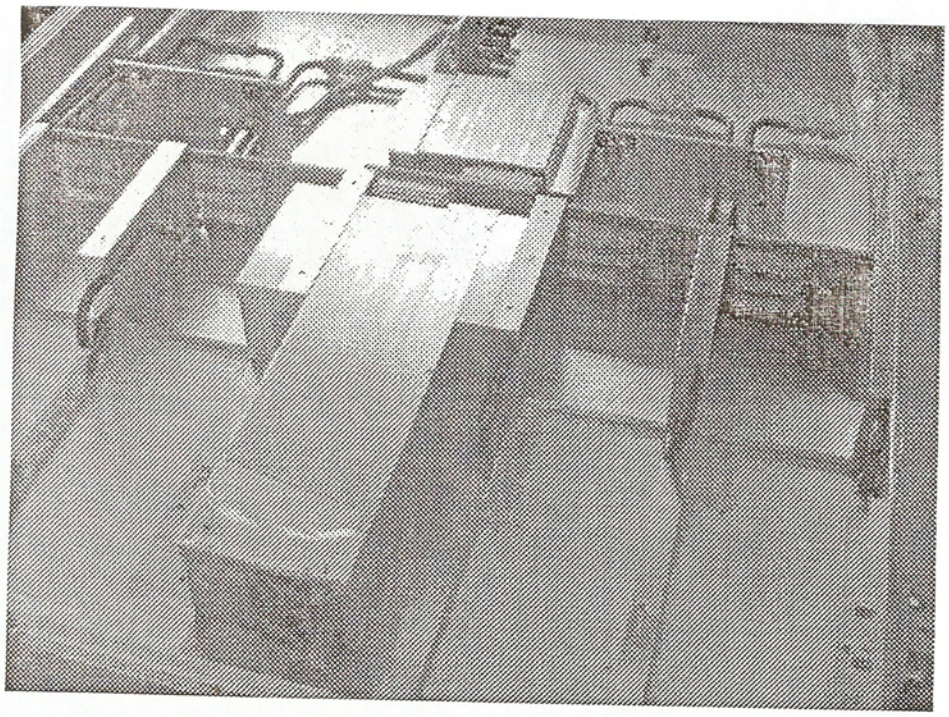


Figure 3.37: Front view of shell of the readout electronics box

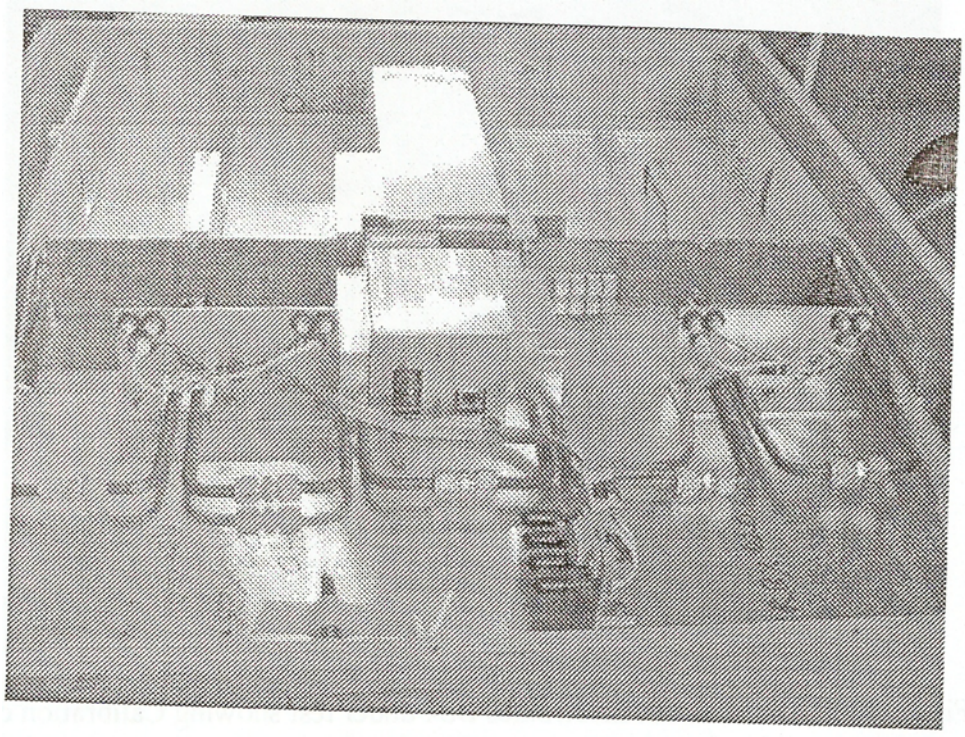


Figure 3.38: Back view of shell of the readout electronics box

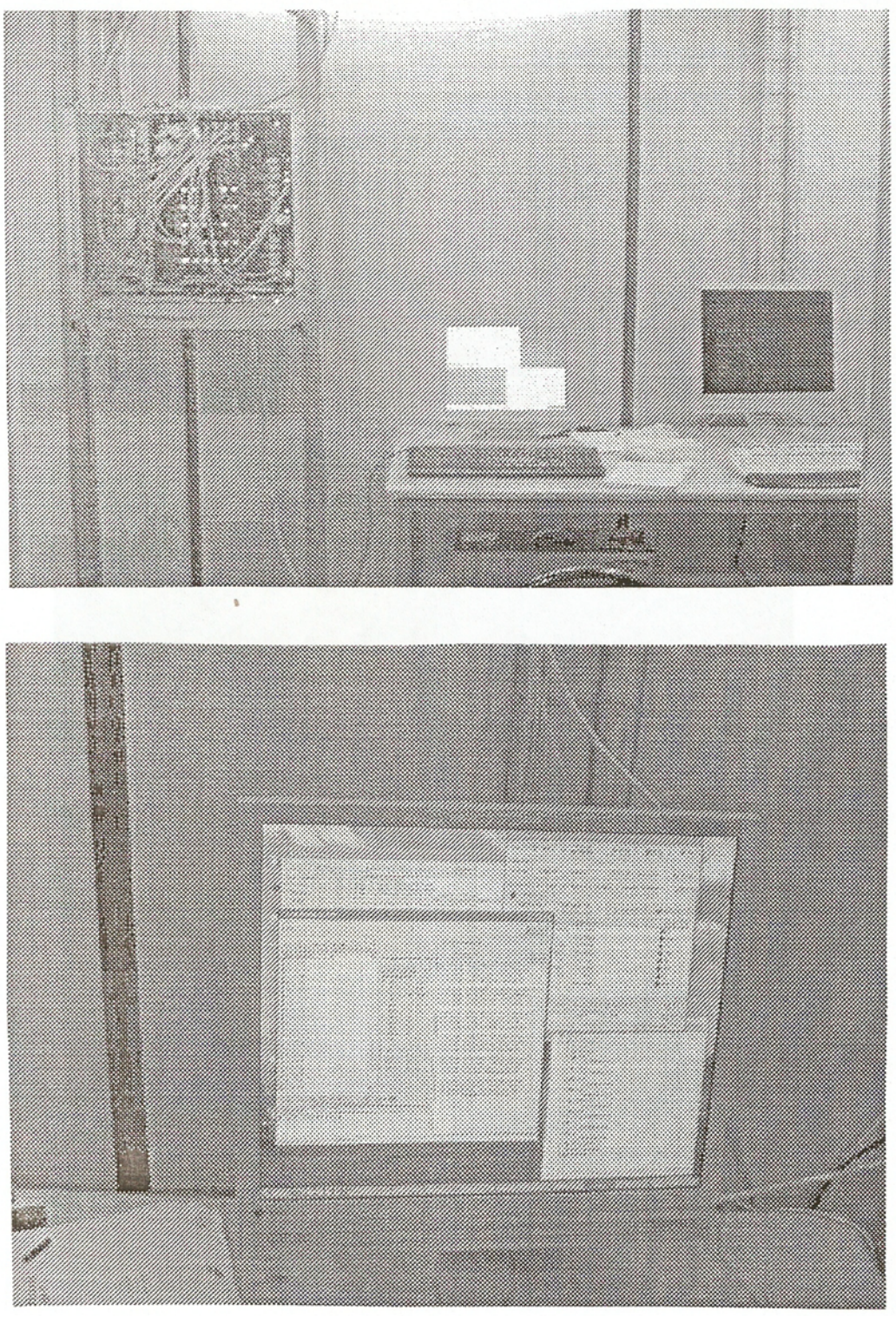


Figure 3.39a: Test Stand for Readout Electronics Box (picture 1 and 2)

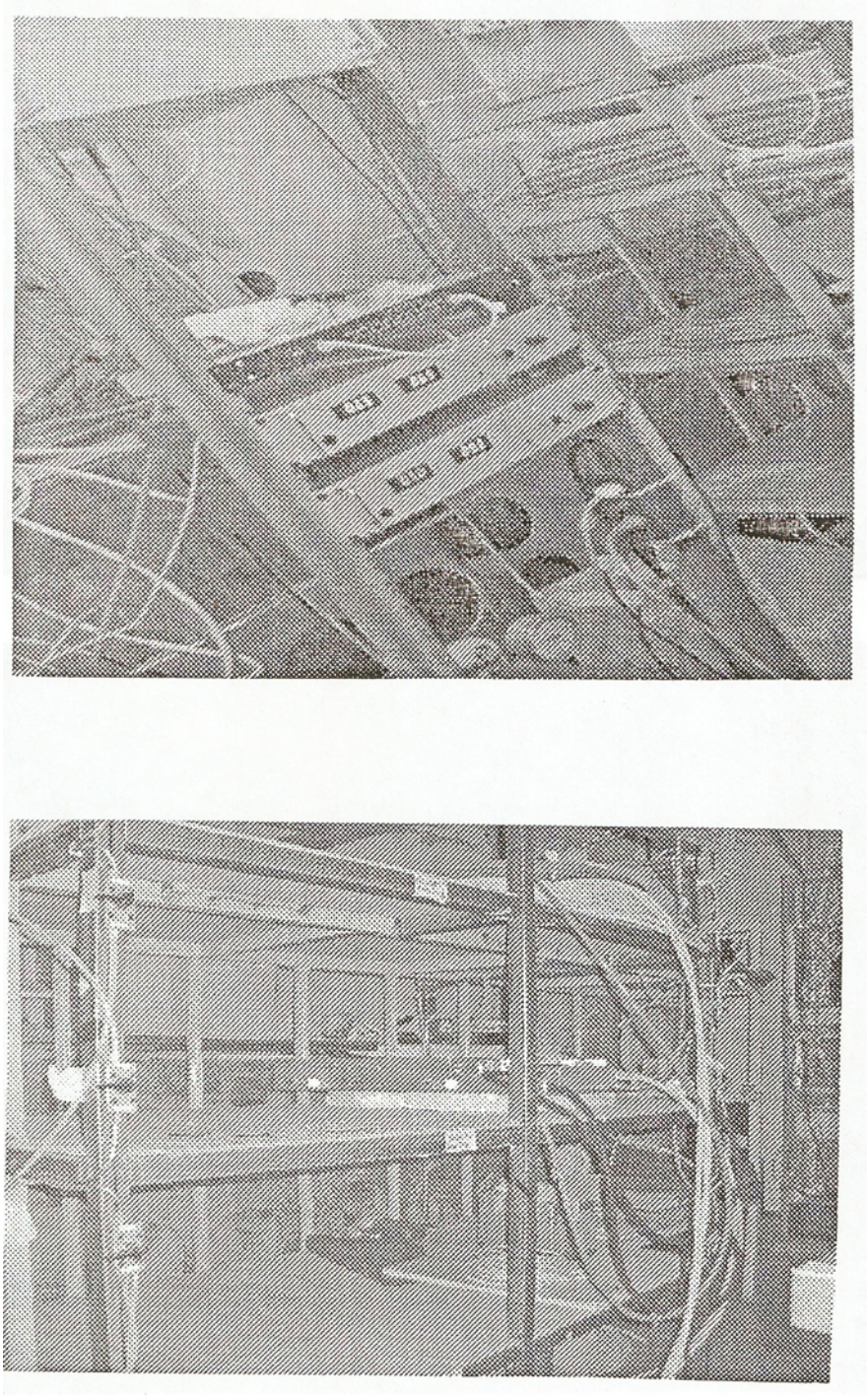


Figure 3.39b: Test Stand for Readout Electronics Box (picture 3 and 4)

## *CHAPTER 5:*

## *BASICS OF ELECTRICITY AND ELECTRONICS [15] [16] [17]:*

Electronics in this fast developing society has now become the most important branch of engineering. We talk of electronics in almost all industry today. Electronics gadgets and equipments are largely being used in all fields like e.g. medicine, communication, defense, automobile industry, computers, data analysis, and research in science &technology. There is hardly any area left where electronics is not playing its roll. It is therefore a formidable challenge to all today and some basics fundamentals to be understood. The purpose of this chapter is to get oneself familiarized with some basics of both electricity and electronics to work with various electronic modules and instruments for the required application.

## 5.1 ELECTRICITY:

Electricity is an invisible force. The force is the attraction or opposition between charges. Electricity is flow of electrons in a conductor. The principal behind the flow of electrons through a wire is the potential difference between the charges. We have positive and negative terminals on a battery. If we were to attach a wire to one end of a battery and bring it closer to the other end of the battery, as soon as we were close enough where the potential difference (Voltage) was able to overcome the resistance of the air, electrons would flow or attract and we would have a spark. Electrons with a path to travel will be attracted to the opposite terminal and repelled from the alike.

### 5.1.1 VOLTAGE:

It is a measure of the work needed to move an electrical charge. We can also say that voltage is a force. We use V as symbol for voltage. E is the symbol used for Electromotive force (e.m.f.).

### 5.1.2 CURRENT:

Current is the movement of electrons through a conductor and is expressed as ampere A. The more flow of current greater the current.

### 5.1.3 RESISTANCE:

Resistance is opposite to the current flow. Every medium has a resistance and resistance of the substance is determined by the nature of the substance, of which it is composed, the dimensions of the object, and the temperature. This is known as resistivity. Rsistivity is expressed in terms of ohms resistance per cubic centimeter at $20^{o}$ C ($68^{o}$ F). Light bulbs. Motors, electric heating elements and relay coils all have resistance even though they are just wires.
Resisters are in general cylindrical in shape with a lead at either end.

Types of Resistors:

1. *Composite type resistors*: The conducting material used in this type of resistors is carbon.
2. *Metal film resistors*: usually consists of metal or metal oxide on a ceramic substrate. There power setting is confined to 3W.
3. *Wire wound resistors*: These consist of wire of alloy wound between terminals on supporting Ceramic, Nicrome or Maganisium is used as alloy wire typically.
4. *Variable resistors*: It is a mechanical rider which rides over the resistance element thus selecting the length of the element to be included in any circuit.

Figure 5.1 illustrate the color coding for resistance value of each unit for four band resistors. Numerical value associated with each color is given in the table below.

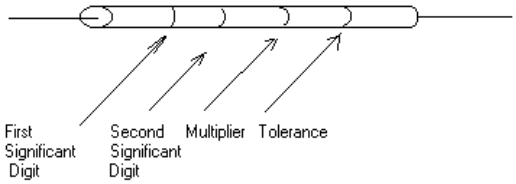



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Figure 5.1: Color Coding Bands Arrangement

| Color | Significant Digit | Multiplier | Tolerance |
|---|---|---|---|
| Black | 0 | $10^0$ | - |
| Brown | 1 | $10^1 = 10$ | - |
| Red | 2 | $10^2 = 100$ | - |
| Orange | 3 | $10^3 = 1000$ | - |
| Yellow | 4 | $10^4 = 10000$ | - |
| Green | 5 | $10^5 = 100000$ | - |
| Blue | 6 | $10^6 = 1000000$ | - |
| Violet | 7 | $10^7 = 10000000$ | - |
| Gray | 8 | $10^8 = 100000000$ | - |
| White | 9 | $10^9 = 1000000000$ | - |
| Gold | - | $10^{-1} = 0.1$ | 5% |
| Silver | - | $10^{-2} = 0.01$ | 10% |
| No Color | - | - | 20% |

There are resistance bands at one end. The first and second band gives the first and second digit of resistance value. The third color band gives the multiplicity factor and the last gives the tolerance factor.
e.g.

Yellow Violet Orange Silver = $47X10^3 \pm 10$ % tolerance
Resistances color coding for 5 band resistors is explained below in figure 5.2.
Sequence of color code is:

BLAC, BROWN, RED, ORANGE, YELLOW, GREEN, BLUE, PURPLE, SILVER, WHITE

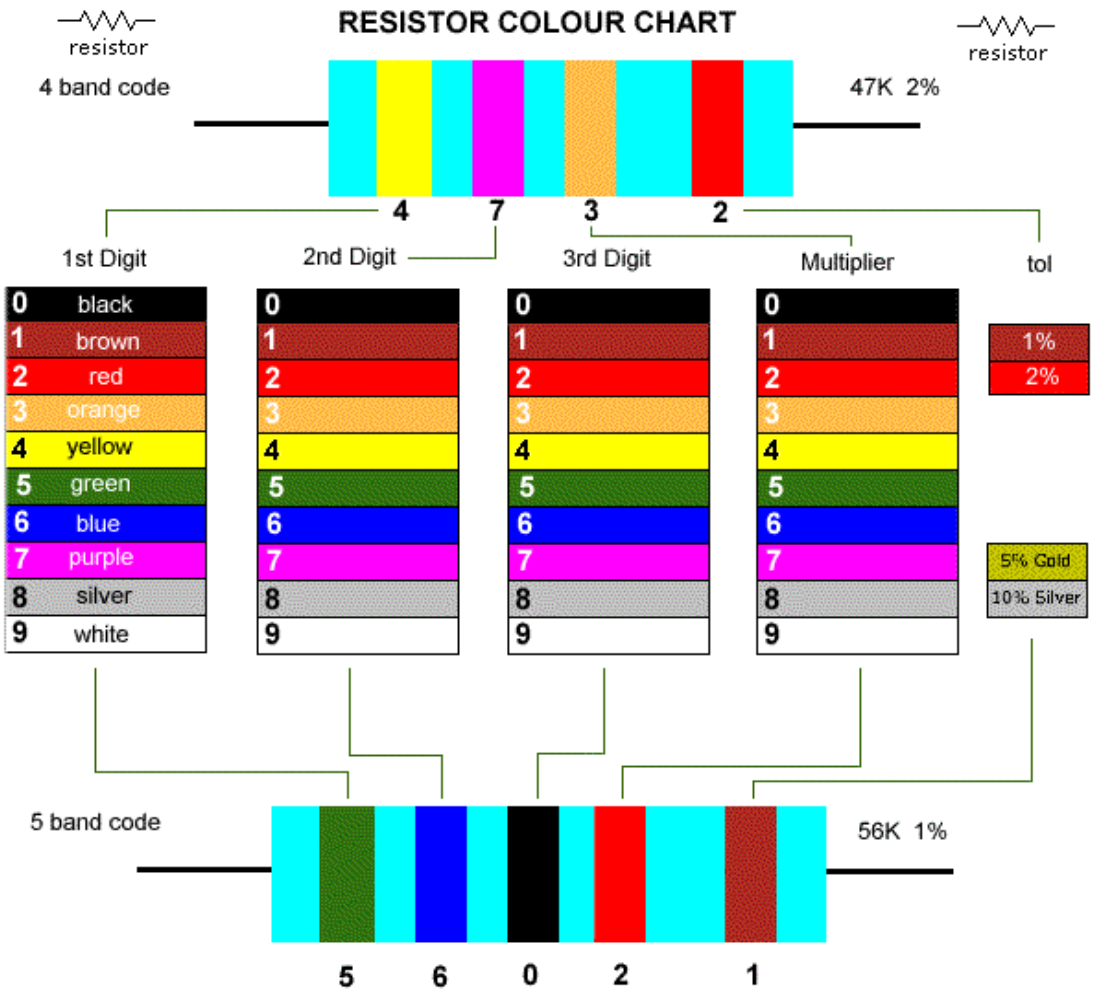



Figure 5.2: Resistance color chart code

The five band color code is more likely to be associated with more precision 1% and 2% types. 5% general purpose type will be four band resistance codes.

## 5.1.4 OHM'S LAW:

This is the most basic law of current flow and is named after its discoverer George Ohm. It states that the amount of current flowing through a circuit is directly proportional to Voltage and inversely proportional to the amount of resistance in a circuit. What does this all mean: if we increase the voltage in a given circuit and resistance stays same the current will increase, or if the voltage is same and we increase the resistance the current will drop.

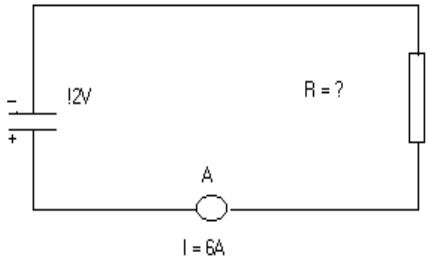
Formula:

# E = I X R

E = Voltage
I = Current also known as A or amps
R = Resistance also known as ohm

Ohms law can be applied to both AC and DC circuit. However AC involves inductances and capacitances and becomes complex to understand ohms law. It is therefore better to talk about DC to understand ohms law. DC is current that flows in one direction.

For understanding let us consider the following circuit:




When everything is connected the ampere meter gives a reading of 6 amps. Now how to find out the unknown resistance in the circuit?

**E = I X R**

**E = 12 Volts, I = 6 amps & R = ?**

**Or**

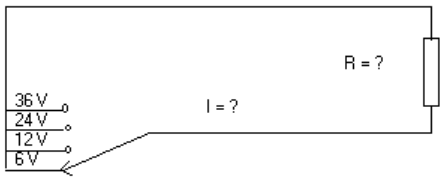
**12 = 6 X R**

**R = 12/6**

**R = 2 ohms**

If in the above example we were to double the voltage to 24 volts, the resistance would be

**R = 2 ohms**




Look at the figure above and answer the following question for practice:

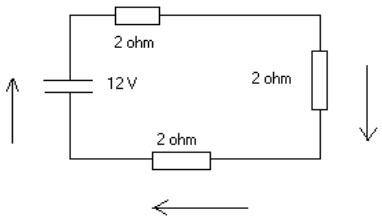
1. 6V power supply and we add a light bulb with a resistance 4 ohm. What will our current be?
2. 12V powers supply and we measure a current reading of 8 amps. What will be our resistance?
3. 24V power supply and relay with a resistance of 6 ohm. What will be the current?
4. 36V power supply and current drawn is 10A. What will be the resistance?
5. We have a heater with resistance of 8 Ohms and the power requirement on the name plate is 120V.What will the current be?

Answer: 1- 1.5A 2- 1.5 ohms 3- 4 amps 4- 3.6 ohms 5- 1 amps

## 5.1.5 TYPES OF CIRCUITS:

- **Series Circuits:**
  A series circuit is a circuit where there is only one for the current to flow. Therefore current in series circuit is always the same. The net resistance of the Such circuits in series are calculated as follows:

**R1 +R2 + R3 = R Total**

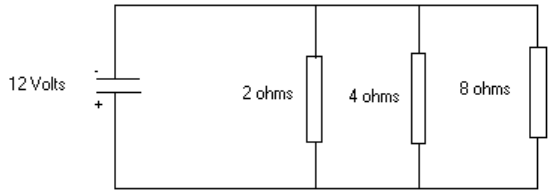



R = R1 + R2 + R3

R = 6
V = 12
I = ?
Answer I = 2 A

- **Parallel Circuits:**
  In parallel circuit the loads are arranged to allow the positive terminals to be joined to a single conductor and all the negative one to the another conductor so that the current travels through different parallel path. The total resistance of a parallel circuit is reciprocal of the sum of the reciprocals of each resistor.

**R total =** $\dfrac{1}{\frac{1}{R1}+\frac{1}{R2}+\frac{1}{R3}}$

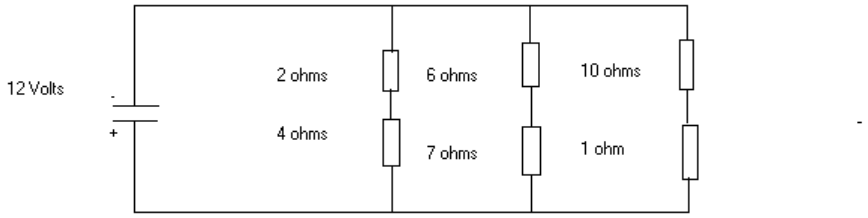



Total resistance in the above circuit will be as follows:

**1/R total = 1/2 + 1/4 + 1/8 = 7/8**
**And R will be 8/7 = 1.143 ohms**

- **Series Parallel Circuit:**

These circuits have both series and parallel branches in them. They are bit complicated but can easily be worked out.




We break such circuit into smaller ones. In the above circuit we have parallel Branches and each parallel branch have 2 resisters in series with other. Let us first combine the series resisters so that we have in all three branches.
Path A = 3+4 = 7 ohms
Path B = 6+7 = 13 ohms
Path C = 10+1 = 11 ohms
As you can see now all we have to worry about is the parallel circuit
1/R total = 1/7 + 1/13 + 1/11 = 311/1001 = 3.219 ohms

## 5.1.6 POWER:

It is the measure of the amount of energy produced or used by a circuit per unit time. When current flows through a resister it produces heat. This heat is evidence that some energy is being used. This is how a fuse opens because of resultant heat produced by excessive current. It melts the metal link and opens the fuse.

Power is expressed in Watts or V/A

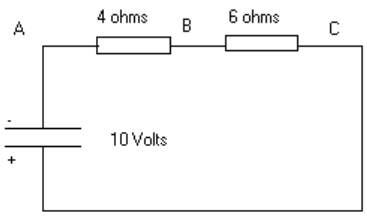
Example: The wattage of a 40VA transformer is 40 watts

**P = I X E**

Where P is power I the current and E the voltage

## 5.1.7 VOLTAGE DROP:

With current I through a resistance, by ohms law the voltage across R is equal to I X R.




I = 1 A, R = 4 + 6 = 10, V = 10 Volts So that I = 10/10 = 1 amp
Since total voltage in the circuit is 10 Volts which applied across total resistance of 10 ohms therefore the current is 1 amp.
Now we know the current through the circuit, we can find out voltage drop across each resistor:
V1 = I X R1, 1 amp X 4 ohms = 4V Voltage drop of 4 volts from A to B
V2 = I X R2, 1 amp X 6 ohms = 6 V Voltage drop of 6 volts from B to A
Total voltage drop = 10 Volts
The IR voltage across each resistor is called the voltage drop. Total of all voltage drops in the circuit shall equal to the supply voltage

## 5.1.8 CAPACITORS:

A capacitor is an arrangement for string large amount of electric charge and hence electric charge in a small space. It consists of two parallel metal conducting plates separated by an insulating material. When a voltage is applied across the plates, an equal and opposite charge appears on the plates and hence no net flow of electric charge occurs but only displacement takes place which is known as polarization.

We name C as storing capacity or capacitance of a capacitor which is given by

$$\mathbf{C} = \frac{Q}{V}$$

Q is the charge and V is the voltage across the capacitor. The symbol of a capacitor ⊣⊢ is:

## A very important property of Capacitors:

Capacitors are used to store energy in the form of an electric field, producing an ac voltage drop and passing high frequencies while rejecting low frequencies. No current flows through the capacitor if a direct current is applied across it. But when an ac voltage is applied across, it is alternatively charged and discharged in each cycle. Figure 5.3 explains the capacitors passing ac and blocking dc.

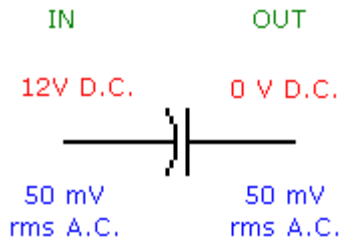



Figure 5.3: Capacitors passing ac blocking dc

## Functional explanation of the Capacitor:

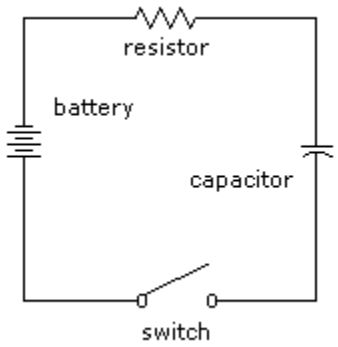



Figure 5.4: Capacitor Schematic in a Circuit

In this circuit drawn in figure 5.4, when the switch is open the capacitor has no charge upon it, when the switch is closed current flows because of the voltage pressure, current is determined by amount of resistance in the circuit. At the instance the switch closed the emf forces electrons into the top plate of the capacitor from negative end of the battery and pulls others out of bottom plate towards the positive end of the battery.

Two points are to be considered here. Firstly as current flow progresses more electrons flow into the capacitor and greater opposing emf is developed there to oppose further current flow, the difference between battery voltage and the voltage on capacitor becomes less and less and current continues to decrease. When the capacitor voltage equals the battery voltage no further current will flow.

The second point is if the capacitor is able to store one coulomb of charge at one volt, it is said to have a capacitance of one Farad. This is a very large unit of measure. Power supply capacitors are often in the region of 4,700 $\mu$F or 4,700/ millionth of a Farad. Radio circuits often have capacitances down to 10 pF which is 10/ million.

## Capacitors in Series and parallel:

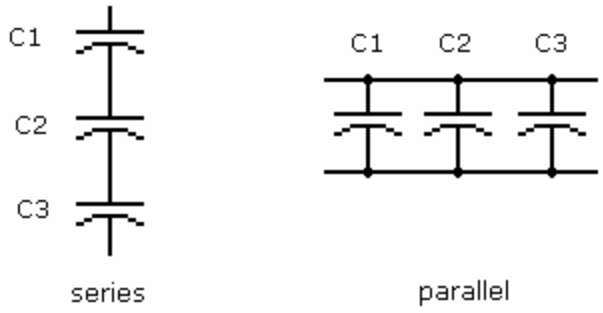



Figure 5.5: Capacitors in series and parallel

Capacitors in parallel add together as C1 + C2 + C3 +……. whereas in series reduce by:
1/ (1/C1 + 1/C2 + 1/C3 + ……)
Consider three capacitors of 10, 22 and 47 $\mu$F respectively.
Added in parallel we get 10 + 22 + 47 = 79 $\mu$F. While in series we would get:
1/(1/10+1/22+1/47) = 5.997 $\mu$F

## What do capacitors look like?

Capacitors vary according to size, application and environmental conditions under which they are used. The main variable element is the dielectric which stores the charge. The types of plates also differ depending upon application.

Depending upon the dielectric in use the capacitors are divided into 4 main groups:

1. Electrolytic capacitors
2. Paper capacitors
3. Plastic capacitors
4. Ceramic capacitors

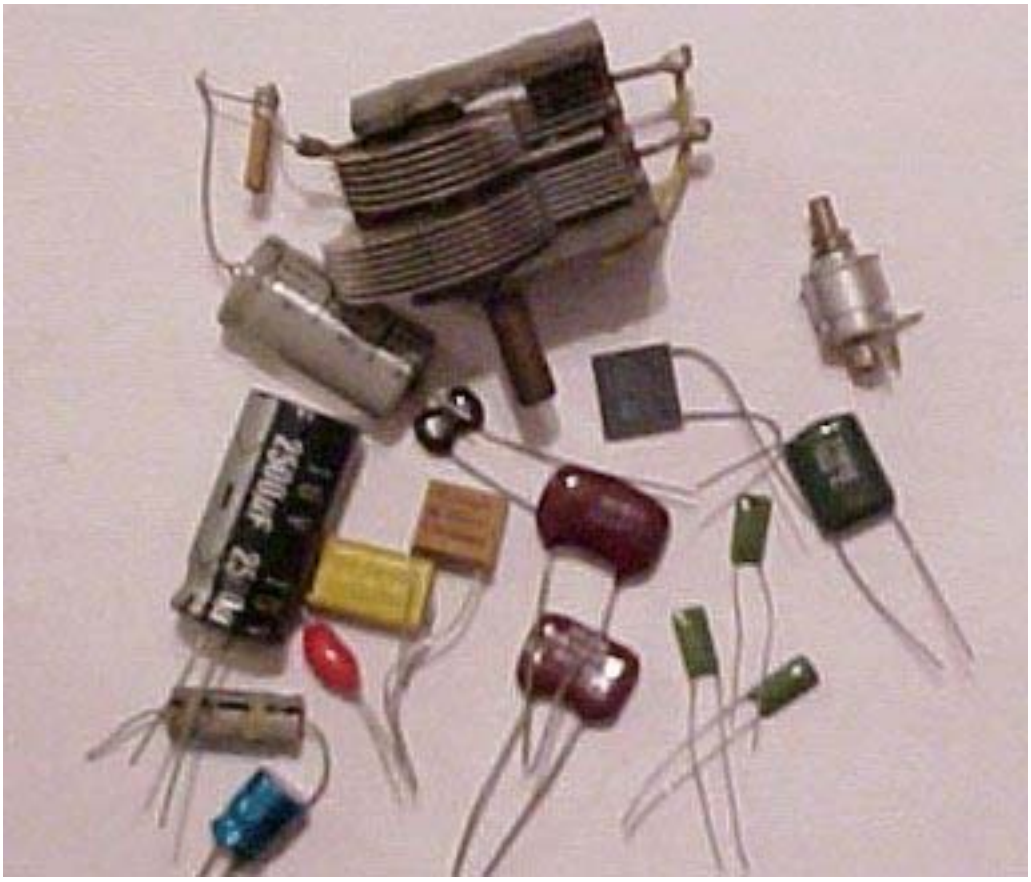


Figure 5.6: A Selection of fixed and variable capacitors

Photo in figure5.6 shows selection of fixed and variable capacitors. The upper capacitor is variable capacitor. Down left hand we have number of electrolytic capacitors.

The red Capacitors in the lower left is a tag tantalum type of greater tolerance and high stability. The yellow is metallised polypropylene film type while the green ones at the right are the popular polyester type “Greencapes”.

In the middle are silver mica capacitors. At upper right is 25 pF beehive trimmer.

## Capacitor Identification Code:

There are no international agreements in place to standardize capacitor identification. Most plastic film types (Figure 7) have printed values and are normally in microfarads or if the symbol is n, Nan farads. Working voltage is easily identified. Tolerances are upper case letters: M = 20%, K = 10%, J = 5%, H = 2.5% and F = ± 1pF.

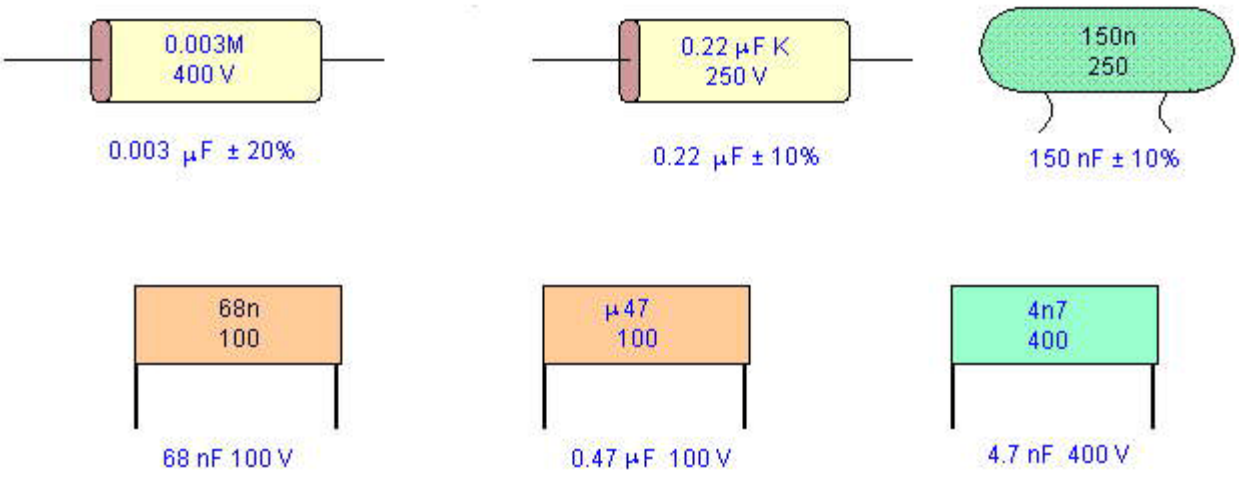



Figure 5.7

A more difficult scheme is shown in Figure 2 with examples. The unit is Pico farads and the third number is a multiplier. A capacitor coded 474K63 means 47 × 10000 pF which is equivalent to 470000 pF or 0.47 microfarads. K indicates 10% tolerance. 50, 63 and 100 are working volts.

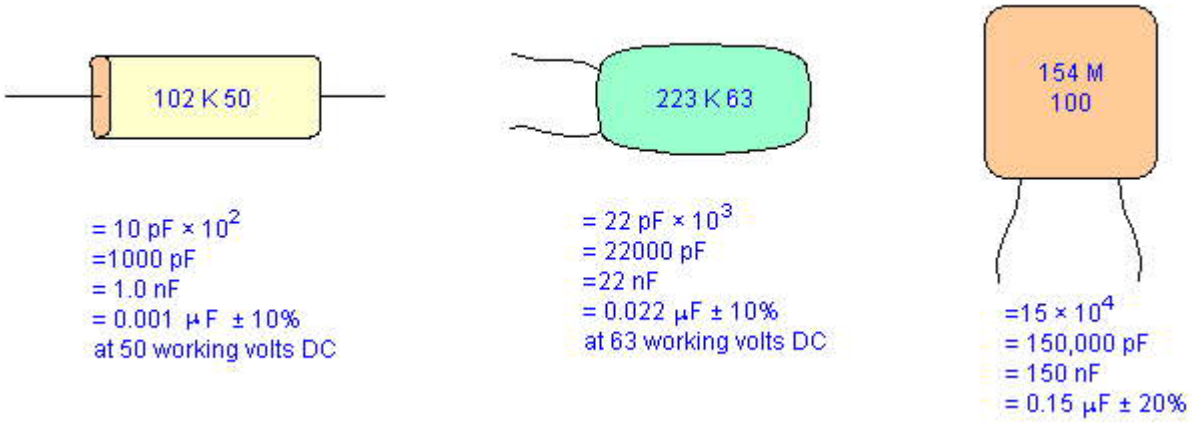



Figure 5.8

Ceramic disk capacitors have many marking schemes. Capacitance, tolerance, working voltage and temperature coefficient may be found. See Figure 9. Capacitance values are given as number without any identification as to units. (uF, nF, pF) Whole numbers usually indicate pF and decimal numbers such as 0.1 or 0.47 are microfarads. Odd looking numbers such as 473 is the previously explained system and means 47 nF.

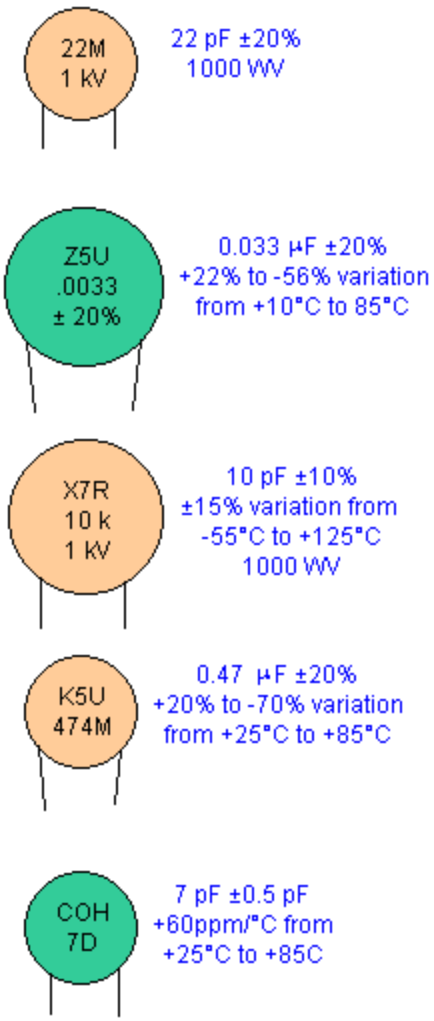



Figure 59

## 3.1.9 INDUCTANCE:

The property of inductance might be described as “when any piece of wire is wound into a coil form it forms an inductance which is the property of opposing any change in current”. Alternatively it could be said “inductance is the property of a circuit by which energy is stored in the form of an electromagnetic field’.
The standard value of inductance is the HENERY, a large value of which like Farad for Capacitance is rarely encountered in electronics today. Typical values of units encountered are millihenery mH, one thousandth of hennery or the micohenery $\mu$H, one millionth of a hennery.
A small straight piece of wire exhibits inductance (probably a fraction of $\mu$H) although not of any significance unit until we reach UHF frequencies.
The value of inductance varies in proportion to the number of turns squared.

**Inductance Formula:**

**Imperial measurements**

$$L = r^2 \text{ X } N^2 / ( 9r + 10 \text{ len} )$$

Where:

L = inductance in $\mu$H

N = number of turns

Len = length of the coil in inches

**Metric measurement**

$$L = 0.394\, r^2 \text{ X } N^2 / ( 9r + 10 \text{ len} )$$

Where:

L = inductance of in $\mu$H

r = coil radius in centimeters

N = number of turns

Len = length of the coil in centimeters

## Solenoid Inductors:

Coils wound on a former (with or without core) may have multilayer of windings which are called solenoid windings.

## Self Resonant Frequency of an Inductance:

All coils also exhibit a degree of self capacitance caused by minute capacitances building up around and between adjacent windings. This self capacitance combined with the natural inductance will form a resonant circuit (self resonant frequency) limiting the useful upper frequency of the coil. There are special winding techniques to be used on occasion to minimize this self capacitance.

## Iron Core:

If the coil is wound on an inductance is greatly increased and the magnetic lines of force increase proportionally. This is the basic of electromagnets.

## Power transformers:

When a coil is wound on special iron laminator or core and a second winding is placed on the core a "transformer" results. This is the basic of all transformers although only alternating current ( a.c. ) can be transformed. The voltage relationship in transformer is proportional to the turns. For example a power transformer might have 2,500 turns on primary side and secondary side might have 126 turns. Such a relationship is 250 : 12.6 and if the primary were connected to 250V a.c. the secondary would produce a voltage of 12.6V a.c.

Interestingly, if the ore size and the wire diameter on the primary supported a primary current of 100 mA. The primary power available would be 250V X 100 mA or 250 X 0.1 = 25 watts. Ignoring core and copper losses we could say that a 25 watt is now available on secondary side at 12.6V which is 25 / 12.6V = 1.98 amp. In practice we don't get that kind of efficiency however it would pay to remember that most power transformers are designed to function most efficiently at or near full design load.

## R.F. Transformers:

In many radio applications coil is wound on a ferrite or powdered iron core. Typical examples are ferrite rod receiving antenna used in cheep transistor radios or the i.f. transformers enclosed in metal cans in those radios – red, yellow, black, green cores. The core is manufactured to be optimum for frequency range of interest and greatly enhances the inductance for specific number of turns. If we wound a coil on a blank former we might get an inductance of say 10 $\mu$H, adding a specific core might inductance to 47 $\mu$H. By using screw in / screw out core ( as in the metal cans ) we can vary the inductance over a fair range of interest.

## 3.1.10 REACTANCE:

Reactance is the property of resisting or impending the flow of ac current or ac voltage in inductors and capacitors. We talk of alternating current only and not of direct current.

## Inductive Reactance:

When ac current flows through an inductor a back emf or voltage develops opposing any change in initial current. This opposition or impedance to change in current flow is measured in terms of inductive reactance.
Inductive reactance is determined by the formula:

$$2 * pi * f * L$$

where: 2*pi = 6.2832; f = frequency in hertz and L = inductance in Henries

## Capacitive Reactance:

When ac voltage flows through a capacitance an opposing change in initial voltage occurs, this opposition or impedance to change in voltage is measured in terms of capacitive reactance.
Capacitive reactance is determined by formula:

$$1 / ( 2 * pi * f * C )$$

where: 2*pi = 6.2832; f = frequency in hertz and C = capacitance in Farads.

## 5.1.11 TRANSFORMERS:

When two coils are placed in closed proximity to one another the line of force from one cut across the turns of the other inducing an ac current, energy is transformed from one winding to another and this is called transformer action.

**Power transformers:**

Power transformer translates voltage from one level to another. Schematic is shown in figure 10 below. Power transformers are used in power supplies.

Figure 5.10: Transformer Schematic

Some transformers have centre tap on the secondary side. The left hand side in the figure 10 denotes “primary” whilst the right hand side is denoted to “secondary” side of a transformer. Most of the power transformers are designed in the region of 50 /60 Hz which is principal frequency around the world. Some examples of power transformers are shown in figure 11.

Figure 5.11: Different types of transformers

The transformer on the upper left has “flying leads” , and is 240V-6.3V CT transformer.
The upper right one is multi tape type with flying leads on both sides. The output allows you to select 6, 3V, 9V, 12V and 15V depending upon the requirement, maximum current is 1A.
On the bottom left is a “plug pack” transformer used in Australia. It is plug in type to mains and has also rectifiers built in. It is a 12V DC with 1 A at the output.
The bottom right one is a multi-tape type transformer.

**Audio Transformer:**

Essentially the main purpose of an interstage audio transformer is to isolate the D and couple the signal, with minimal loss. The transformer windings look like short circuits to DC, yet are seen as complex impedances to AC signals. Much which contained on the topic of audio transformers is of necessity somewhat over simplified to give general view.

**RF Transformers:**

RF falls into two categories, band pass filters and broad band transformers. Band pass filters might well fall into category of those used in IF amplifier circuits while broad band transformers are generally used for impedance matching.

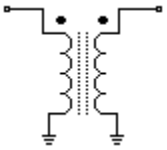


Figure 5.12: Schematic of an RF transformer

Broad band RF transformer schematic is shown in figure 5.12. It is often wound on a ferrite toroid of sufficient permeability to give reactance of about 5 times the highest impedance at lowest frequency of interest.

## 5.2 DIODES :

Diodes are semiconductor devices which might be described as passing current in one direction only. Diodes can be used as voltage regulators, tuning devices in rf tuned circuits, frequency multiplying devices in RF circuits, mixing devices in rf circuits, switching circuits or can be used to make logic decisions in digital electronic circuits. There are also diodes which emit light which are known as “Light Emitting Diodes” or LED’s. We can say diodes are extremely versatile.

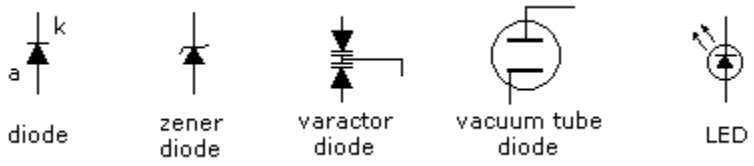



Figure 5.13: Schematic symbols for diodes

### 5.2.1 SEMICONDUCTORS:

Semiconductor is a material whose electrical conductivity lies in between that of a conductor and insulator. Ge and Si are most commonly used semiconductors. When isolated, Ge and Si atoms have four valence electrons. Semiconductor materials are classified into two types:

- Intrinsic
- Extrinsic

**Intrinsic Semiconductors:**

Pure semiconductors are referred to as intrinsic semiconductors. All the valence electrons are tightly bound to parent atom and to the neighboring atom by covalent bonding. They are not free to move anywhere in the crystal and hence do not conduct electricity. This happens at absolute zero temperature.

A silicon crystal behaves different from an insulator because of any temperature above zero, there is a finite probability that an electron in lattice will be knocked loose from its position, leaving behind an electron deficiency called “hole”.

If voltage is applied, then both the electrons and holes can contribute to a small current flow.

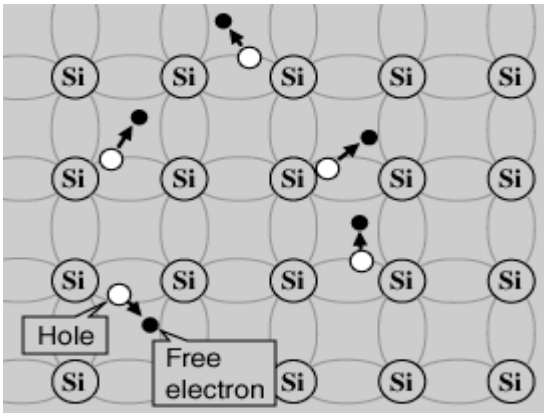



Figure5.14: Electrons and holes

The conductivity of a semiconductor can be modeled in terms of the band theory of solids. The band model of a semiconductor suggest that at room temperature there is a finite possibility that electrons can reach the conduction band and contribute to electrical conduction. The electrons which become free from atomic forces are capable of producing current if potential difference is applied across the semiconductor material.

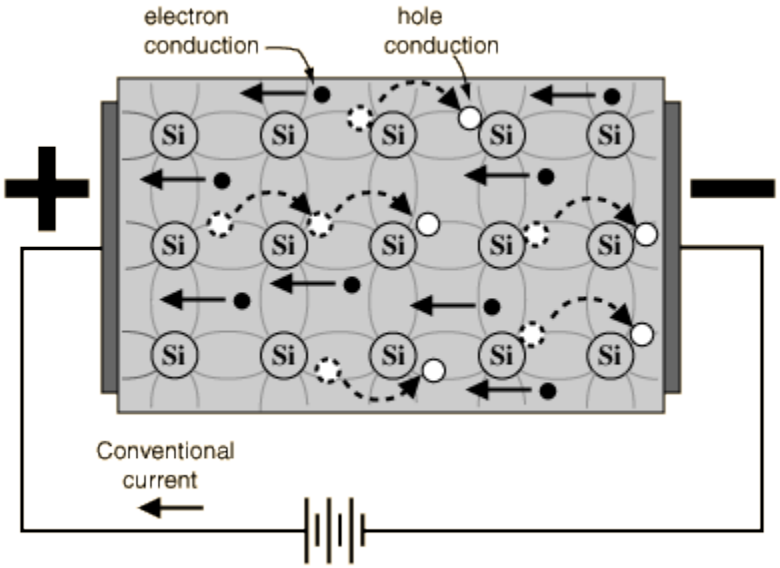



Figure 5.15: Semiconductor Current

The current which flows through the intrinsic semiconductor consists of both electron and hole current That is, the electrons which have been freed from their lattice positions into conduction band can move through the material.

In addition, other electrons can hope between lattice position to fill the vacancies left by the freed electrons. This additional mechanism is called hole conduction because it is as

if the holes are migrating across the material in the direction opposite to the free electron movement.
In a pure crystal of silicon or germanium equal number of electrons and holes are created by heat energy. The free electrons randomly move throughout the crystal. Sometimes it approaches the hole, gets attracted and falls into the hole. This merging of free electrons and holes is called recombination.

**Extrinsic Semiconductor (The Doping of Semiconductors):**

The addition of a small percentage of foreign atom in a regular crystal lattice of silicon or germanium produces dramatic changes in their electrical property, producing n-type and p-type semiconductors. The process of adding impurity is called doping. The doped semiconductor is referred to an extrinsic semiconductor.

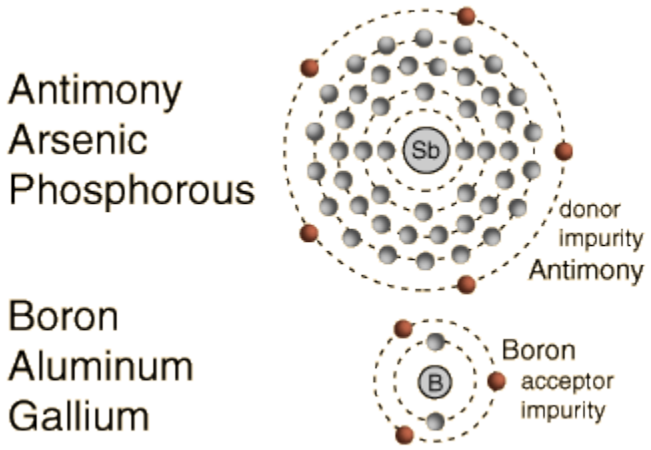



Figure 5.16: Impurities for doping semiconductor

Impurity atoms with 5 valence electrons produce n-type semiconductors by contributing extra electrons.
Impurity atoms with 3 valence electrons produce p-type semiconductors by producing a “hole” or electron deficiency.

**N-Type Semiconductors:**

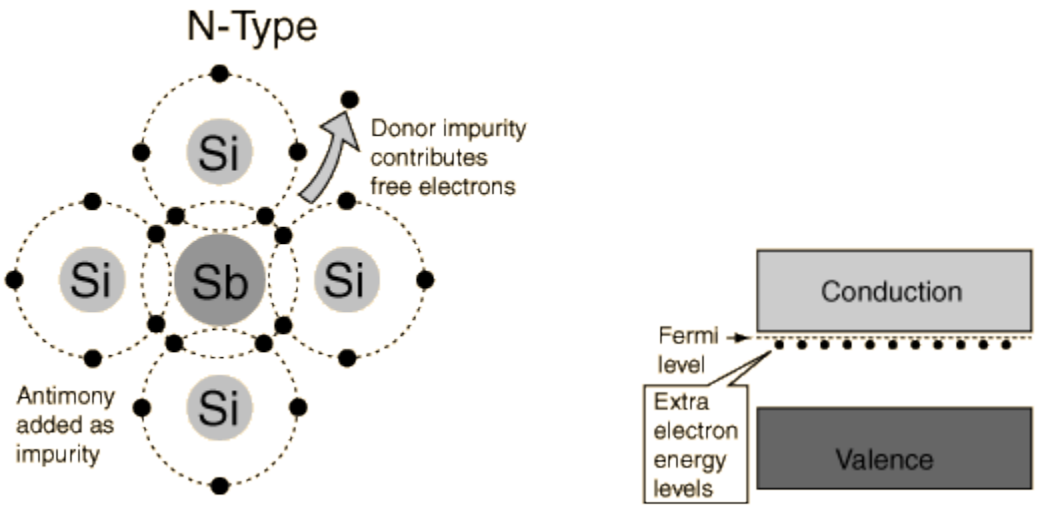



Figure 5.17: N-type Semiconductor

The addition of pentavalent impurities such as antimony or phosphorous contributes free electrons, greatly increasing the conductivity of intrinsic semiconductor. Phosphorous may be added by diffusion of phosphine gas (PH3)

**P-Type Semiconductors:**

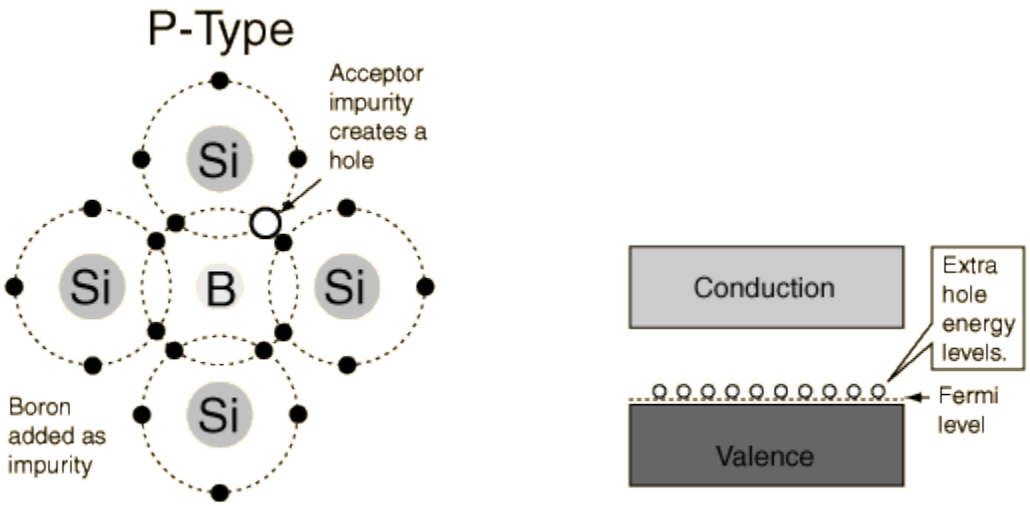



Figure 5.18: P-type semiconductor

The addition of trivalent impurities such as boron, aluminum or gallium to an intrinsic semiconductor creates deficiency of valence electrons, called “holes”. It is typical to use $B_2 H_6$ diborane gas to diffuse boron into the silicon material.
The application of the band theory to n-type and p-type semiconductors show that extra levels have been added by impurities. In n-type material there are electron energy levels near the top of the band gap so that they can be easily excited into conduction band. In p-type material, extra holes in the band gap allows excitation of valence band electrons, leaving mobile holes in the valence band.

## 5.2.2 P-N JUNCTION:

The nature of P-N junction is a crucial key to solid state electronics. When p-type and n-type material is suitable joined together, the junction behaves very differently than either type of material alone. The contact surface is called P-N Junction. Most semiconductor devices contain one or more P-N junction.

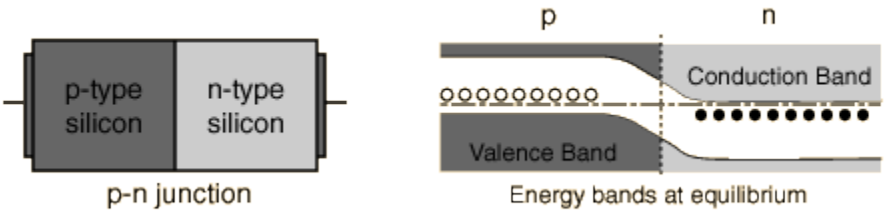



Figure5.19: P-N Junction and Energy Bands

The open circles on left side of the junction in figure represent “holes” or deficiencies of electrons in lattice which can act like positive charge carriers. The solid circles on right of the junction represent the available electrons from n-type dopant. Near junction electrons diffuse across to combine with hoes, creating a depletion “region”. The energy level sketch in the figure is to visualize the equilibrium condition of P-N junction. The upward direction in the diagram represents increasing electron energy.

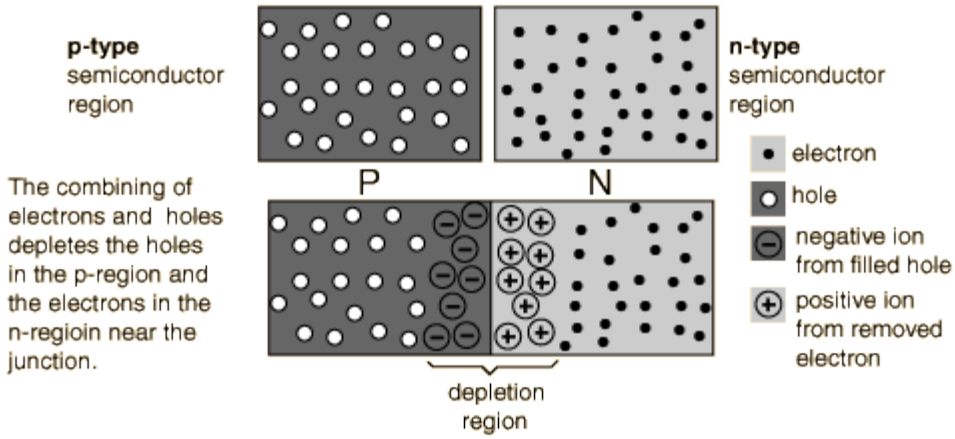
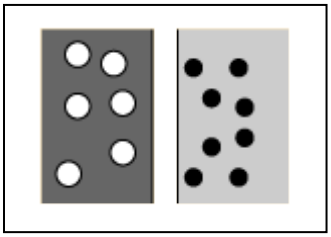
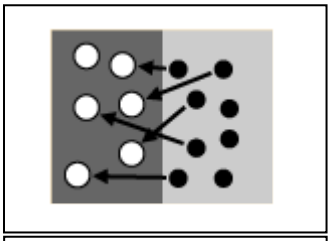



Figure 5.20: Depletion Region in P-N junction

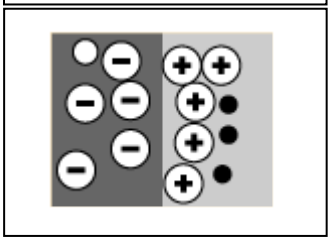
When a P-N junction is formed, some of the free electrons in the n-region diffuse across the junction and combine with holes to form negative ions. In so doing they leave behind ions at the donor impurity sites.



In the p-type region there are holes from acceptor impurities and in the n-type region there are extra electrons.



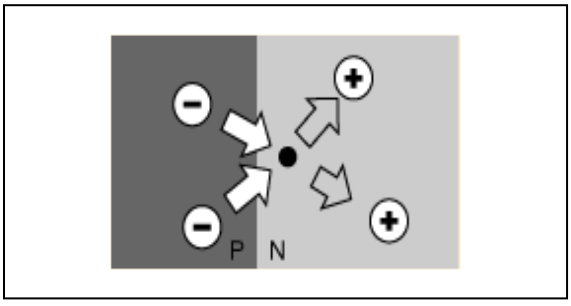
When a p-n junction is formed, some of the electrons from the n-region have reached the conduction band and are free to diffuse across the junction and combine with holes.

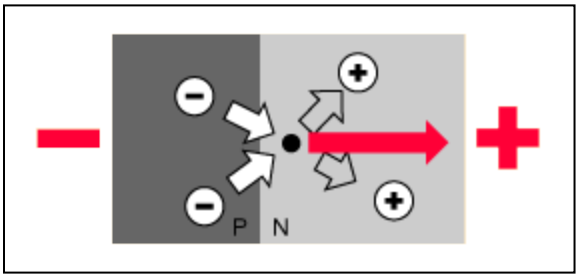


Filling a hole makes a negative ion and leaves behind a positive ion on n-side. A space charge builds up, creating a depletion region which inhibits any further electron transfer unless it is helped by putting a forward bias on junction.

● Electron ○ Hole ⊖ Negative ion from filling of p-type vacancy. ⊕ Positive ion from removal of electron from n-type impurity.

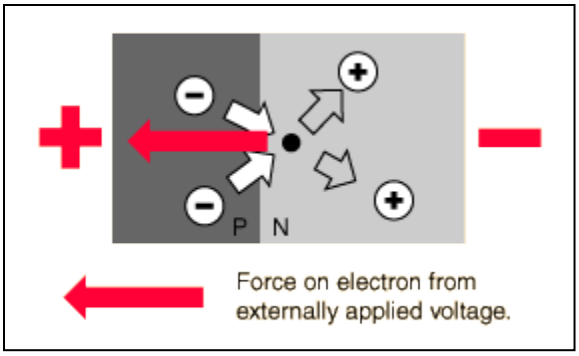
## Equilibrium of junction:



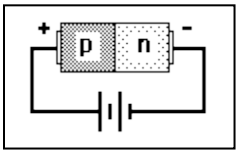

Coulomb force from ions prevents further migration across the p-n junction. The electrons which had migrated across from the N to P region in forming of the depletion layer have now reached equilibrium. Other electrons from N region cannot migrate because they are repelled by the negative ions in region and attracted by the positive ins in the N region.

An applied voltage with the indicated polarity further impedes the flow of electrons across the junction. For conduction in the device, electrons from N region must move to the junction and combine with holes in P region. A reverse voltage drives the electrons away from the junction, preventing conduction.




An applied voltage in the forward direction as indicated assists electrons in overcoming the coulomb barrier of the space charge in depletion region. Electrons with very small resistance will flow in the forward direction.

## Forward Biased P-N Junction:




Forward biasing the p-n junction drives holes to the junction from p-type material and electrons to the junction from the n-type material. At the junction the electrons and holes combine so that a continuous current can be maintained.

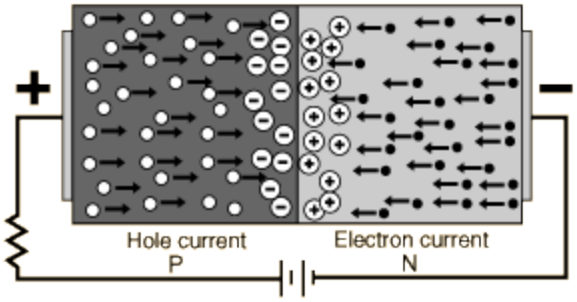
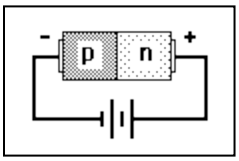



Figure 5.21: Forward Biased P-N Junction

To Apply forward bias, connect positive terminal of battery to p-type and negative to n-type as shown in figure 5.21. The holes are repelled from positive terminal of the battery and are compelled to move towards the junction. The electrons are repelled from the negative terminal of the battery and drift towards the junction. Because of their acquired energy, some of the holes and free electrons penetrate the depletion region. This reduces the potential barrier. The width of the depletion layer reduces and so does the barrier height. So more majority carriers diffuse across the junction. These carriers recombine and cause movement of charge carriers in space-charge region.

For each recombination of free electrons and holes that occurs, an electron from negative terminal of the battery enters the n type material. It then drifts towards the junction. Similarly in the p-type material near the positive terminal of the battery, an electron breaks a bond in the crystal and enters the positive terminal of the battery. For each electron that breaks its bond, a hole is created. This hole drifts towards the junction. The current in p-type material is due to the movement of holes. The current in n-type material is due to the movement of electrons. The current continues as long as the battery is connected in circuit. The forward current through a P-N junction is due to the majority carriers produced by the impurity.

## Reverse Biased P-N Junction:




The application of a reverse voltage to the p-n junction will cause a transient current to flow as both electrons and holes are pulled away from the junction. When the potential formed by the widened depletion layer equals the applied voltage, the current will cease accept for small thermal current.

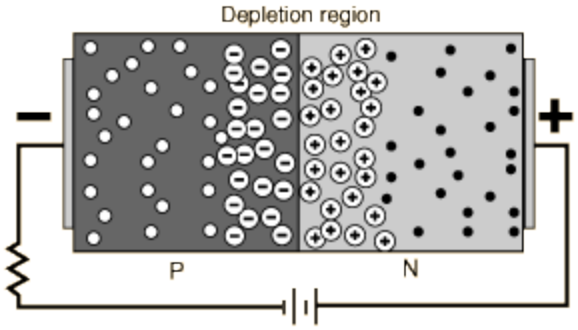


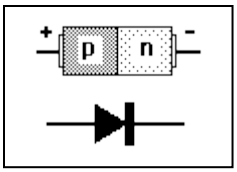

Figure 5.22: Reverse Biased P-N junction

The negative terminal of the battery is connected to the p-type material and the positive to the n-type material. The holes in the region are attracted towards the negative terminal of the battery. The electrons in the n-region are attracted to the positive terminal of the battery. Thus the majority carriers are drawn away from the junction. This action widens the depletion layer and increases the barrier potential.

The increased barrier potential makes it more difficult for majority carriers to diffuse across the junction. This barrier is helpful to the minority carriers in crossing the junction. As soon as minority carriers are generated it is swept across the junction because of the barrier potential. This causes the current flow and is called reverse saturation current. The reverse current is due to the minority carriers produced due to breaking of covalent bonds at room temperature. The flow of current in semiconductor. constituted by the drift of minority carriers which are formed due to external energy supplied is known as “Drift Current”.

The reverse voltage at which p-n junction breaks down with sudden rise in reverse current is called “**Breakdown Voltage**”.

## The P-N Junction Diode:




The nature of p-n junction is that it will conduct in the forward direction but not in the reverse direction. It is therefore a basic tool for rectification in building of DC power supply.

## 5.2.3 V-I CHARACTERISTIC OF A P-N JUNCTION DIODE [16]:

When a diode is connected to a circuit the information about voltage applied across its terminals and current that flows through it is depicted by means of a graph known as V-I characteristics.

P region of a diode is called anode and n-region the cathode. The symbol looks like an arrow pointing from p-region.

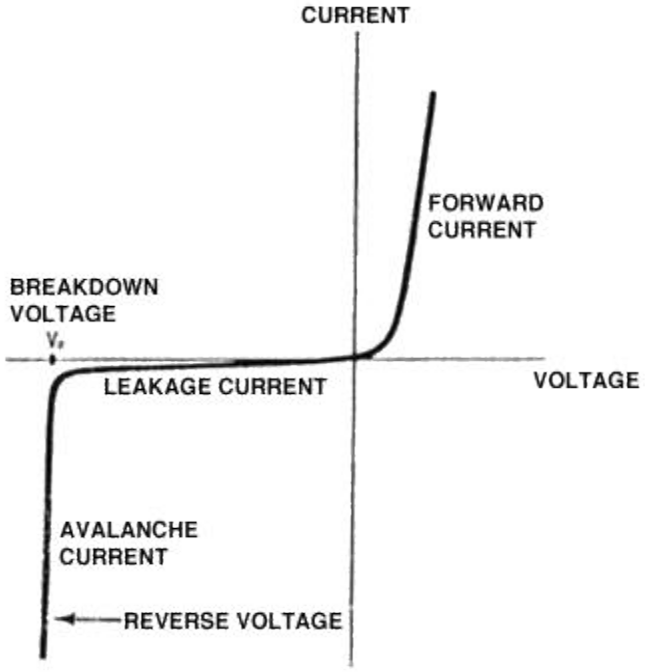



Figure 5.23: V-I Characteristics of a Diode

From the curve in figure 5.25 we find that the diode current in the forward bias is very low for the first few fractions of volts. The diode does not conduct well until the external voltage overcomes the potential barrier. As we approach a particular voltage the diode starts conducting. A small increase in voltage produces a sharp increase in current. The Voltage at which the diode starts to increase current rapidly is called ***Thresh Hold or Knee Voltage.*** It is 0.7 V for Silicone and 0.3 V for Germanium diodes.

In the reverse bias the current is very small. It is only few mA for germanium and a few nA for silicone. It remains small and almost constant for all voltages less than the breakdown voltage $V_z$. At breakdown voltage the current increases rapidly for a small increase in voltage.

The relationship between the current I and voltage V is given by

$$I = I_0 \left( e^{V/\eta V_T} - 1 \right) \qquad \ldots\ldots\ldots \quad (5.1)$$

The positive value of I means that current flows from the p-side to n-side. The diode is forward biased if V is positive, indicating that p-side of junction is positive with respect

to n-side. The symbol $\eta$ is unity for germanium and is approximately 2 for silicon at rated current.
The symbol $V_T$ stands for the electron volt equivalent of temperature and is given as

$$V_T = \frac{T}{11.600} \qquad \ldots\ldots. \quad (5.2)$$

At room temperature ( T+ $300^O$ K)

$V_T$ = 0.026 V = 26 mV.

When the voltage V is positive and several times $V_T$, the unity in the diode equation may be neglected.

$$I = I_0 \in^{V/\eta V_T} \qquad \ldots\ldots\ldots.. \quad (5.3)$$

Accordingly, accept for a small range the neighborhood of origin, the current increases exponentially with voltage When the diode is reverse biased and $|V|$ is several times $V_T$ , I = - $I_0$ . The reverse current is therefore constant, independent of applied reverse bias. Consequently, $I_0$ is referred to as the *reverse saturation current*.
For the sake of clarity the current $I_0$ has been greatly exaggerated in magnitude. Ordinarily, the range of forward current over which a diode is operated is many orders of magnitude larger than the reverse saturation current.
At a reverse biasing voltage $V_Z$, the diode characteristics exhibit an abrupt change in current. At this critical voltage, a larger reverse current flows and the diode is said to be in the *breakdown region.*

**The Cutin Voltage $V_\gamma$ :**

There is a difference in volt ampere characteristic of both silicone and germanium diodes as shown in figure 5.24 . The diodes have comparable ratings. The noteworthy feature in the figure is that there exists a Cutin, offset, breakpoint or threshold Voltage $V_\gamma$ is the forward voltage below which the current is very small. Beyond $V_\gamma$ **,** current rises rapidly. $V_\gamma$ is approximately 0.2 for germanium and 0.6 for silicone.
The cutin voltage of silicone diode characteristic is offset about 0.4 V with respect to the break in the germanium diode characteristic. The reverse saturation current in germanium diode is normally larger by a factor of about 1,000 than the reverse saturation current in silicone diode of comparable rating. $I_0$ is in the range of microampers for germanium diode and nanoamperes for a silicone diode.
Since $\eta$ = 2 for small current in silicone, the current increases as $\in^{V/2V_T}$ for the first several tenths of volt and increases as $\in^{V/V_T}$ only at higher voltages. This initial smaller dependence of the current on voltage accounts for further delay in rise of the silicone characteristics.

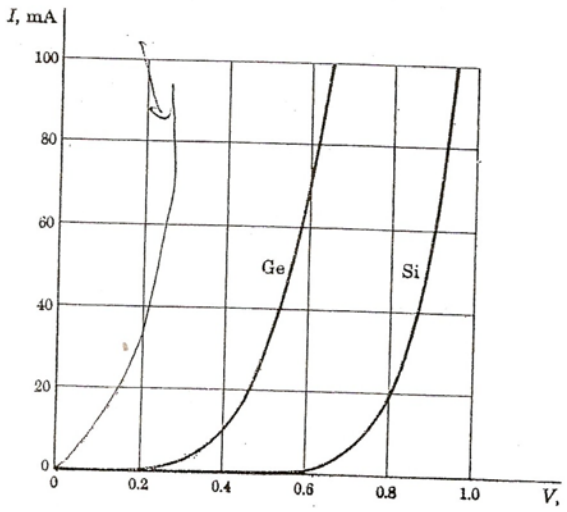



Figure 5.24 The forward volt ampere characteristics of a silicon and germanium diode at $25^0$ C

## 5.2.4 THE TEMPERATURE DEPENDENCE OF P-N CHARACTERISTICS [16] [17]:

Variations in p-n junction may be calculated by equation:

$I = I_0 \ ( e^{V/\eta V_T} - 1 )$ …….. (5.1)

where the temperature is contained implicitly in $V_T$ and also in the reverse saturation current.
The dependence of $I_0$ on temperature is given by:

$I_0 = K T^{2/\eta} \in^{-V_0 / \eta V_T}$ ……. (5.4)

where K is a constant and $eV_0$ is the energy required to break the covalent bond in the semiconductor. For germanium $\eta$ = 1 and $V_0$ = 0.75 V and for silicone $\eta$ = 2 and $V_0$ = 1.12 V.
Taking derivative of the equation we find

$$\frac{1}{I_0}\frac{dI_0}{dT} = \frac{d(\ln I_0)}{dT} = \frac{2}{\eta T} + \frac{V_0}{\eta T V_T} \approx \frac{V_0}{\eta T V_T} \qquad \ldots\ldots\ldots \quad \ldots\ldots\ldots \quad (5.5)$$

since $V_0 / V_T >> 2$.

We deduce from the equation that

$d(\ln I_0)/dT = 0.075/^0 C$ for silicone and 0.10 for germanium.

Since the leakage component is independent of the temperature we expect to find smaller rate of change of $I_0$ with temperature than calculated above.
The reverse saturation current increases approximately 7% / $^0$ C for silicone germanium both.
Now in the equation (5.1) if we drop the unity for constant I in comparison with the exponential, we find,

$$\frac{dV}{dT} = \frac{V}{T} - \eta V_T \left( \frac{I}{T_0}\frac{dI_0}{dT} \right) \approx \frac{V - V_0}{T} \qquad \ldots\ldots\ldots \qquad (5.6)$$

making use of equation 5.5. Consider a diode operating at room temperature and just beyond the threshold voltage V, we find from the equation 5.6

$\frac{dV}{dT}$ = -1.8 mV/$^0$ C for Ge ($V_0$ = 0.75 V) and -1.7 mV/$^0$ C for Si ($V_0$ = 1.12 V) … (5.6)
Since these values are based on average characteristics value can well be taken;

$$\frac{dV}{dT} = -2mV/^0C \qquad \ldots\ldots\ldots\ldots \qquad (5.7)$$

The temperature dependence of forwards voltage is given by the equation 5.6 as difference of two terms. The positive term V/T on the right side results from the temperature dependence of $V_T$. The negative term results from the temperature dependence of $I_0$ and does not depend upon the voltage V across the diode. The equation predicts, accordingly, that at increasing V, dV/dt should become less negative, reach zero at $V = V_0$ and thereafter reverse sign and go positive. This behavior is regularly exhibited by diodes. Normally, however, the reversal take place at current which is higher than the maximum rated current. The curve in figure also suggest this behavior. Reverse characteristics are given in figure 5.25.

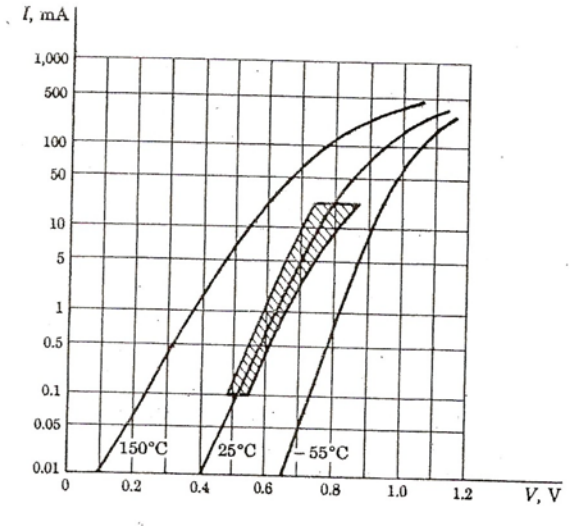



Figure 5.25: Volt Ampere Characteristic at three different temperatures of silicone diode

## 5.2.5 AVALANCHE DIODE OR ZENER DIODE [16] [17]:

Diodes which are designed with adequate power dissipation capacities to operate in the breakdown region are known as Avalanche Breakdown or Zener Diodes. The main application of zener diode is in voltage regulator circuit which holds load voltage constant in spite of change in the line voltage or load resistance.
The reverse voltage characteristic of a diode is drawn in figure 5.26 a and figure 5.26 b shows the manner in which breakdown diode is used as voltage regulator.

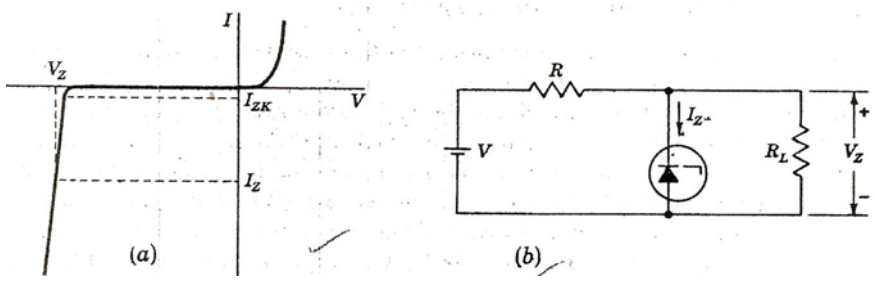



Figure 5.26: (a) Volt Ampere Characteristic of an Avalanche diode
(b) Circuit in which Zener Diode is used as a Regulator

The source voltage V and resistor R are so selected that diode current $I_Z$ is within the specified range and the diode operates in the breakdown region. Here the diode voltage which is also the voltage across the load $R_L$ is $V_Z$ and the diode current is $I_Z$ . The diode will now regulate the load voltage against variations in load current and against variations in supply voltage V because in breakdown region, large changes in diode current produce only small changes in diode voltage. Diode current accommodates, load current or supply current depends upon the power dissipation rating of the diode.
From Kirchoff's current and voltage laws:

$$I = I_Z + I_Z \quad \ldots\ldots\ldots\ldots\ldots(1)$$

And $$V_Z = V - IR \quad \ldots\ldots\ldots\ldots\ldots(2)$$

Also $$V_Z = I_L R_L \quad \ldots\ldots\ldots\ldots\ldots(3)$$

In ideal conditions $V_Z$ remains constant.
Let supply voltage V be kept constant and load current be changed by varying load resistance $R_L$.

Since $\Delta V_Z = 0$ and $\Delta V = 0$, equation (2) yields $\Delta I = 0$
Hence Equation (1) gives

$$\Delta I = \Delta I_Z + \Delta I_L = 0$$

or $\Delta I_Z = - \Delta I_L$

So, when the load resistance is decreased but the supply voltage remains constant the load current $I_L$ increases and zener current $I_Z$ decreases equally so that the supply current I remains fixed.

If on the other hand the load resistance $R_L$ is kept constant and the supply voltage V is changed we find from the equation (2)

$$\Delta V = R \Delta I$$

since $\Delta V_Z = 0$ equation (3) gives $\Delta I_L = 0$ and equation (1) finally yields

$$\Delta I = \Delta I_Z$$

Thus when supply voltage is changed and the load resistance is kept constant the supply current I and zener current $I_Z$ change equally to maintain the load current $I_L$ at a constant value.

Two mechanisms can cause breakdown n a junction diode:

1.Avalanche Breakdown:

At a certain reverse voltage the electric field imparts a sufficiently high energy to thermally generated carriers crossing the junction. The carriers on colliding with crystal ion on its way disrupts the covalent bond and produce a new electron-hole pair. These carriers can also gain sufficient energy from the applied field and collide with other crystal ions to produce further electron-hole pairs. The process is commulative and produces an avalanche of carriers in a very short time. The mechanism known as *avalanche multiplication*, cause a large reverse current as shown by the dashed part of the characteristic. The diode is said to work in the region of *avalanche breakdown*.

2. Zener Breakdown:

Zener breakdown occurs when reverse bias voltage is sufficiently high, so that resulting electric field at the junction exerts a large force on a bound electrons to tear it out of covalent bond. Thus a direct rupture of covalent bonds produce a large number of electrons-hole pair, thereby increasing the reverse current. This process is referred to as *Zener Breakdown.* Unlike avalanche breakdown zener breakdown does not originate from the collision of carriers with crystal ions.

Zener breakdown occurs at voltage below 6V. Nevertheless the term zener breakdown is commonly used for avalanche breakdown even at higher voltages.

Avalanche Diode are available for voltages from several volts to several hundred volts with power ratting up to 50W.

## 5.2.6 TUNNEL DIODES [15] [16] [17];

When the concentration of impurity carriers is very high say 1 part to $10^3$ in both P and N region of a diode the characteristics of a diode completely changes. As depicted in figure 5.27. The width of the junction barrier is reduced from 5 microns to 100 Å.

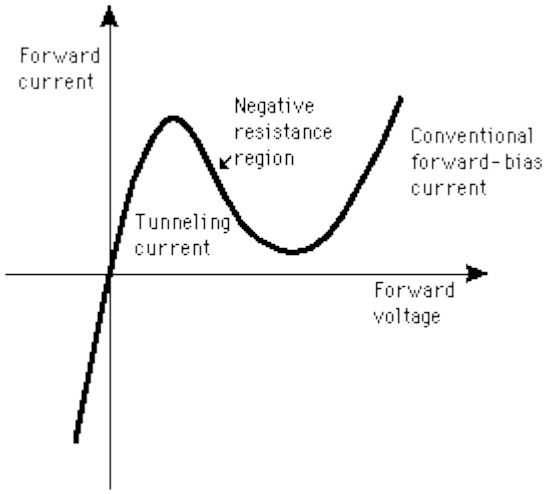



Figure 5.27: Volt Ampere Characteristic of a Tunnel Diode

Classically a particle must have an energy at least equal to the height of a potential barrier if I is to move one side of the barrier to the other. However as the barrier is very thin as stated above, quantum mechanics dictates that there is a large probability that an electron will penetrate through the barrier. The Quantum mechanical behavior is referred to as "tunneling" and hence these high impurity density p-n junction devices are called "tunnel diodes.

As a consequence of the tunneling effect and the band structure of heavily doped semiconductors the volt ampere characteristic of figure 5.26 is obtained. The device is an excellent conductor in the reverse direction. Also a small forward voltage i.e. 50 mV for Ge the resistance remain small (of the order 5 ohm). At the peak current $I_P$ corresponding to voltage $V_P$, the slop dI/dV of characteristic is zero. If V is increased beyond $V_P$ , then the current decreases. As a consequence the dynamic conductance g = dI/dV is negative. The tunnel diode exhibits a negative resistance characteristic between the peak current $I_P$ and minimum value $I_V$ called the valley current. At the Valley voltage $V_V$ at which $I = I_V$ the conductance is again zero, and beyond this point the resistance becomes and remains positive. The current again reaches the value $I_P$. At the so called peak forward voltage $V_F$ the current again reaches the value $I_P$. For larger voltages the current increases beyond this value. The portion beyond $V_V$ is caused by the injection current in an ordinary p-n junction.

For currents whose values are between $I_V$ and $I_P$ the curve is triple valued, because each current can be obtained at different applied voltages. This multi valued feature makes the tunnel diode useful in pulse and digital circuitry. Tunnel Diode is a useful switching device. From the curve it is clear that characteristic is a multi valued function of current, it is a single valued function of voltage. Each value of current corresponds to one particular value of current. Hence the tunnel diode is said to be *voltage controllable*.

## 5.2.7 BACKWARD DIODE [10]:

A tunnel diode which is not so highly doped and has a small peak current and is used in reverse direction is said to be a backward diode. The volt ampere characteristic of such a diode is shown in figure 5.28. As this device is a better conductor in reverse than forward direction it is called a "backward diode" In the reverse diode the current due to tunneling effect is large only in the reverse direction. That is why it is also called "unitunnel diode"

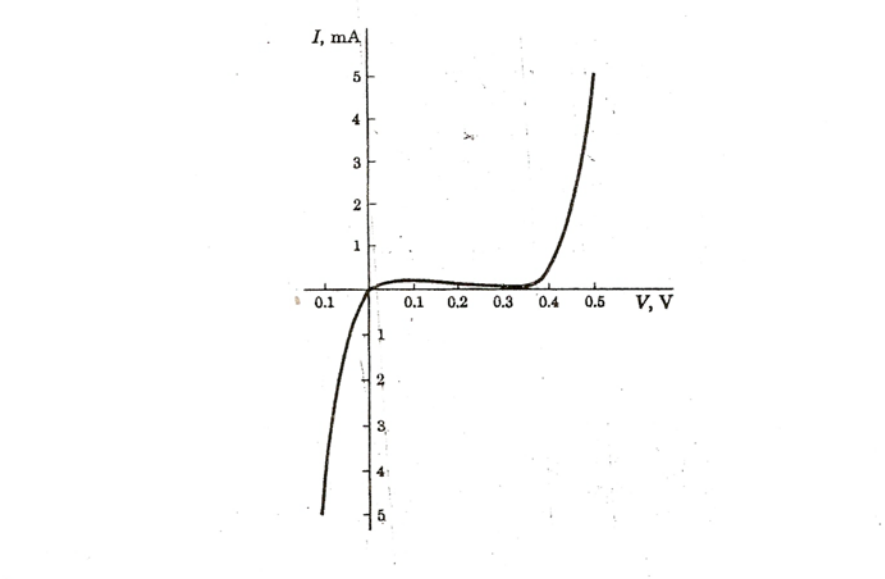



Figure 5.28: A typical germanium backward diode characteristic

The high conduction characteristic is in the third quadrant. Since this characteristic corresponds to the forward conduction in a conventional diode, it is customary to plot the back diode with the voltage and ampere current scale both reversed. In the back diode, the "forward direction" of the applied voltage is actually the direction where p side of the diode is negative with respect to n side. The appearance of the characteristic may be seen as upside down. The temperature sensitivity of the back diode is less than that of a conventional diode. The break point, at room temperature of a back diode is at 0V whereas the break point of a conventional diode is 0.6V to 0.7V. The back diode is therefore very useful when rectifying action of a diode is required in connection with small amplitude waveforms. Suppose, by way of example if a sinusoidal signal is applied to a rectifying circuit which consists of a diode resistor in series. If the signal has an amplitude of say 200mV and diode is conventional, the diode will hardly conduct and rectification will be very poor. With a back diode the efficiency will be greatly improved.

## 5.2.8 THE FOUR-LAYERED DIODE [16]:

The device consists of four layers of silicon doped alternatively with p- or n-type impurities as represented in figure 5.29. Because of this structure it is called a p-n-p-n diode or switch. The terminal p region is the anode, or p emitter, and the terminal N region is cathode, or n emitter.

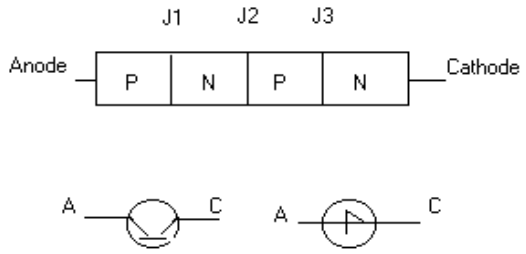



Figure 5.29 A four layered p-n-p-n diode

When an external voltage is applied to make anode positive with respect to the cathode, junction J1 and J3 are forward biased and centre junction J2 is reversed biased. The externally impressed voltage appears principally across the reverse biased junction and current which flows through the device is small. As the impressed voltage is increased, the current increases slowly until a voltage called the forcing voltage or breakdown voltage $V_{BO}$ is reached where the current increases abruptly and the voltage across the device decreases sharply. At this breakdown point the pn-p-n diode switches from OFF to its ON position.

The device can be split as two transistors back to back. One transistor is p-n-p type and the other is an n-p-n type as shown in the figure 5.30.

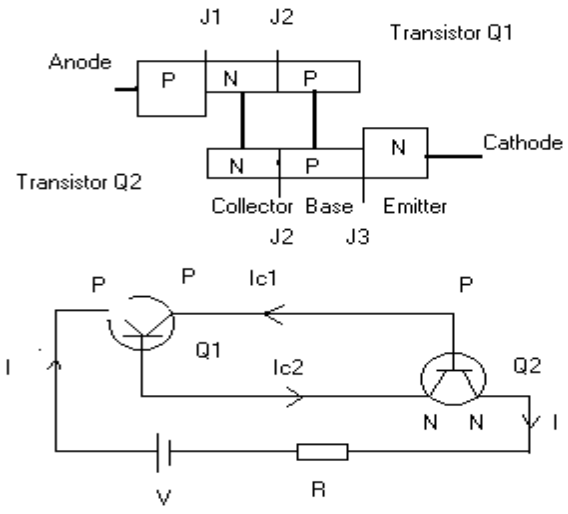



Figure 5.30: The p-n-p-n diode redrawn to make it appear two interconnected "Transistors"

The n region that is the base of transistor is the collector of the other, and similarly for the adjoining P region. The junction J2 is common collector junction for both transistors. In figure 5.29 the arrangement is redrawn using transistor symbols and voltage source has been impressed through a resister across the switch, giving rise to current I. Collector current for transistor Q1 and Q2 are indicated. In active region the collector current is given by:

$I_C = -\alpha I_E + I_{co}$ …… 5-8

With $I_E$ the emitter current, $I_{CO}$ the reverse saturation current, and $\alpha$ the short circuit common base forward current gain. We may apply equation 5-8 in turn to Q1 and Q2. Since $I_{E1} = +I$ and $I_{E2} = -I$, we obtain

$I_{c1} = -\alpha_1 I + I_{co2} = 0$ ……..5-9

$I_{c2} = \alpha_2 I + I_{co2}$ ……5-10

For p-n-p transistor $I_{co1}$ is negative and for n-p-n $I_{co2}$ is positive. Hence we write $I_{co2} = -I_{co1} = I_{co} / 2$. Setting equal to zero the sum of the current into transistors we have

$I + I_{c1} - I_{c2} = 0$ ……5-11

Combining the equations 5-8 through 5-11 we find

$$I = \frac{I_{co2} - I_{co1}}{I - \alpha_1 - \alpha_2} = \frac{I_{co}}{I - \alpha_1 - \alpha_2} \qquad \text{……5-12}$$

We observe that the sum $\alpha_1 + \alpha_2$ approaches unity equation 5-12 indicates that current I increases without limit; that is the device breaks over. This is because of the manner the two transistors are interconnected. The collector current of Q1 is furnished as base current of Q2 and vice versa. When the p-n-p-n switch is operating in such a manner that the sum $\alpha_1 + \alpha_2$ is less than unity, the switch is in its OFF state and the current I is small. When the condition $\alpha_1 + \alpha_2 = 1$ is attained, the switch transfers to the ON state. The voltage across the switch drops to a low value and the current becomes large, being limited by external resistance in series with the switch.

## 5.3 TRANSISTORS [15] [16] [17] [20]:

A Transistor is a three terminal active semiconductor device that provides current amplification. There are two types of transistors:

1. The bipolar junction transistor (BJT)
2. The field effect transistors (FET)

### 5.3.1 BIPOLAR JUNCTION TRANSISTOR:

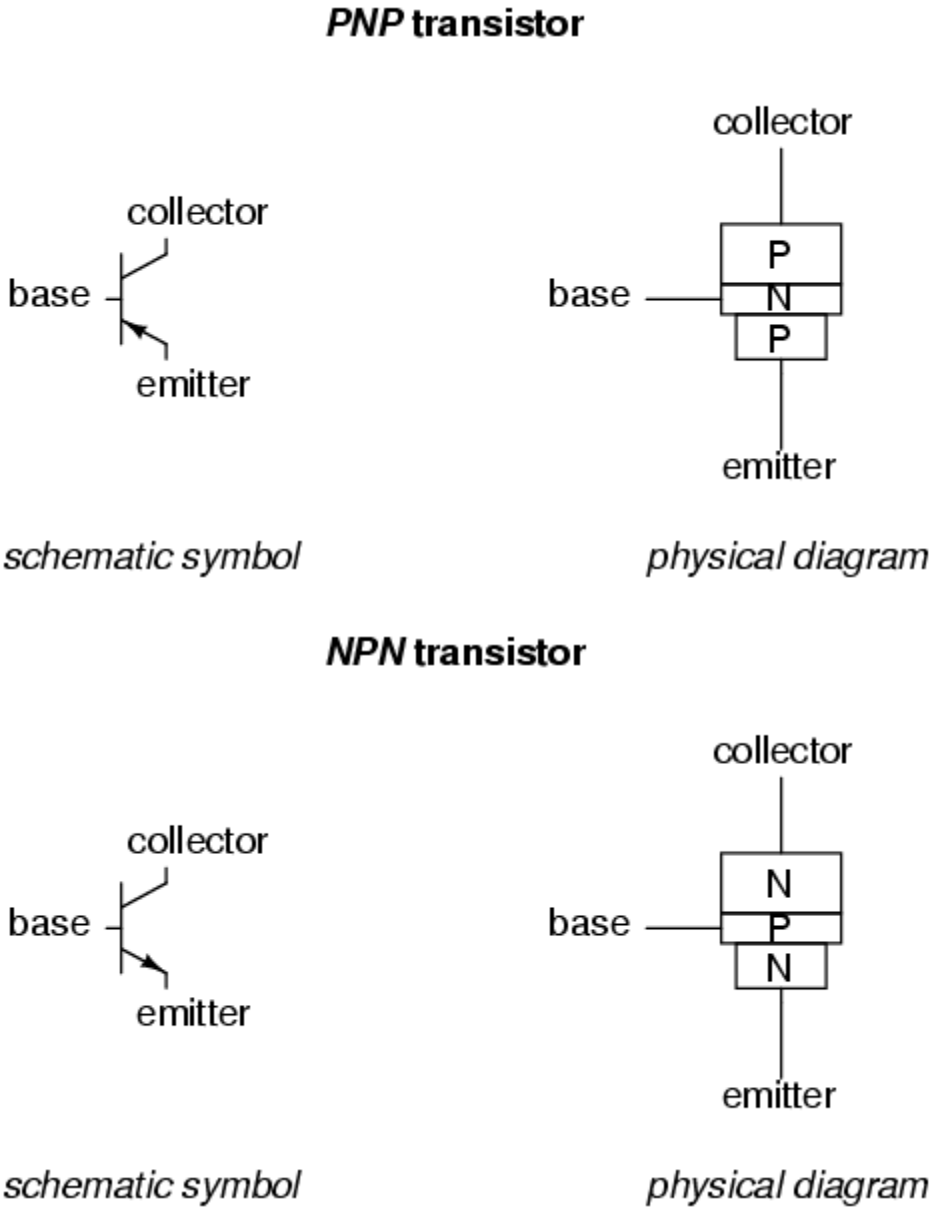
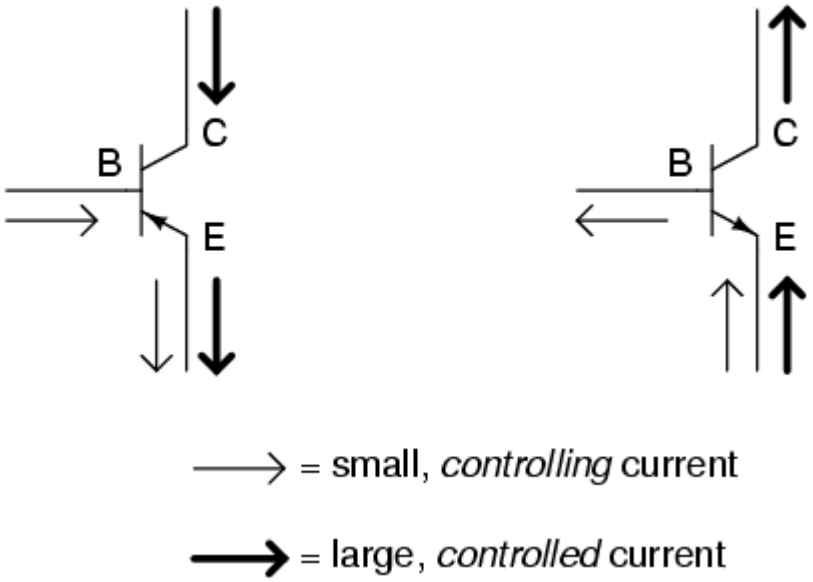



Figure 5.31: Transistor symbols and small transistor package

A bipolar transistor consists of three-layer "sandwich" of doped (extrinsic) semiconductor materials, in two flavors i.e. P-N-P or N-P-N. Each layer forming a specific name and each layer is provided with a wire contact for connection to a circuit. The schematic symbols and physical diagrams of these two transistor types is shown in figure 5.31. The difference between NPN and PNP is the proper biasing (polarity) of the junctions when operating. For any given operation the current direction and voltage polarity for each type is exactly opposite to each other.

Bipolar transistors work as a current regulator. In other words they restrict the amount of current that can go through them according to a smaller, controlling current. The main current that is controlled goes from collector to emitter, or from emitter to collector, depending on the type of transistor it is (PNP or NPN respectively). The small current that controls the main current goes from base to emitter or from emitter to base, once again depending upon the type of transistor it is. According to the confusing standards of semiconductor symbology, the arrow always points against the direction of electron flow.




A transistor is called bi-polar because the main flow of electrons through them takes place in two types of semiconductor material: P and N, as the main current go from emitter to collector or vice versa. In other words, the two types of charge carriers—electrons and holes –comprise this main current through the transistor.

The controlling current and the controlled current always mesh together through the emitter wire, and their electrons always flow against the direction of the transistor's arrow. This is the first and foremost rule in the use of transistors: all the current must be going in proper direction for the device to work as a current regulator. Small controlling current is usually referred to as base current and the large controlled current is referred to as the collector current. The emitter current is the total of the base current and collector current.

***Properties that meet the rules for npn transistors (for pnp simply reverse all the polarities) are*:**

1. The collector must be more positive than emitter
2. The base emitter and base collector behave like diodes (figure 5.32). Normally base emitter diode is conducting and base collector is reverse biased, i.e. the applied voltage is in the opposite direction to easy current flow.

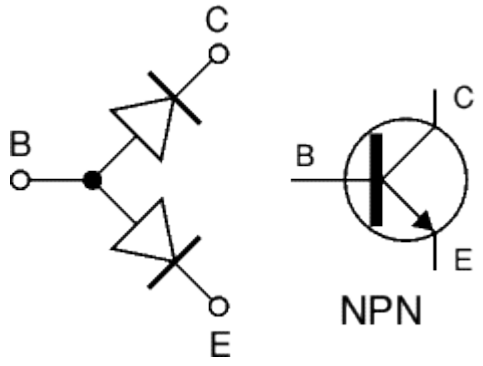


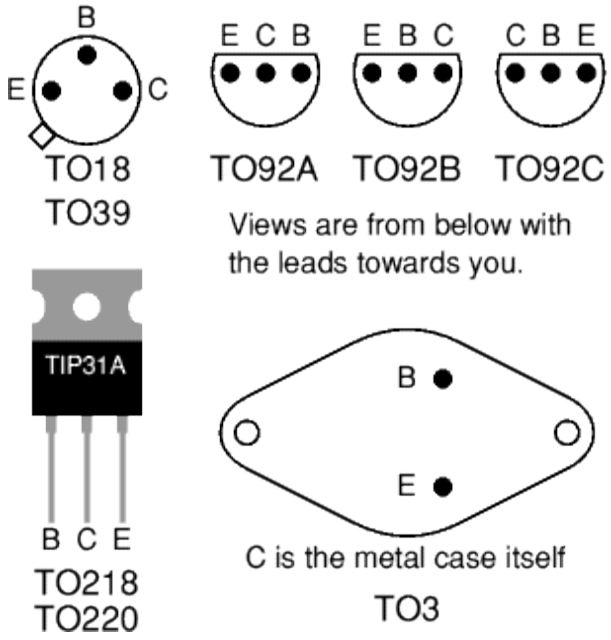

Figure 5.32: An ohm meters view of transistor terminals

3. Any given transistor has maximum values of $I_C$, $I_B$, and $V_{CE}$ that cannot exceed. Also There are other parameters like power dissipation temperature and $V_{BE}$ etc which one should keep in mind.
4. When rule three is obeyed, $I_C$ is roughly proportional to $I_B$ and can be written as $I_C = h_{FE}I_B$ - $\beta I_B$ where $h_{FE}$, the current gain also called beta is typically about 100. Both $I_C$ and $I_E$ flow to emitter. The collector current is not due to forward conduction of the base collector diode; that diode is reverse biased.

Property 4 gives the transistor its usefulness; a small current flowing into the base controls a much larger current into the collector.

Note particularly the effect of 2: We can't go sticking a voltage across the base-emitter terminals, because an enormous current will flow if the base is more positive than emitter by more than 0.6 to 0.8 volts (forward diode drop). This rule also implies that an operating transistor has $V_B \sim V_E + 0.6V$ ( $V_B = V_E + V_{BE}$). Polarities are given for npn transistor; reverse them for pnp.

We should not think that the collector current as diode current. It is not because collector base diode normally has voltages applied across it in the reverse direction. Collector current varies very little with collector voltage.




The Drawing on the right shows the leads of most common case styles in transistors. The transistor lead diagrams show the view from the below with the leads towards you.

Figure 5.33: Transistor leads for some common transistors

## 5. 3. 2 STRUCTURE AND PRINCIPLE OF OPERATION [19]:

A bipolar junction transistor consists of two back-to-back p-n junctions, who share a thin common region with width, $w_s$. Contacts are made to all the three regions, the two outer regions called the emitter and collector, and the middle region called the base. The structure of an npn bi-polar transistor is shown in figure 5.34 (a).

The sign convention of the current and voltage is indicated on figure 5.34 (b). The base and collector current are positive if a positive current goes into the base or collector contact. The emitter current is positive for a current coming out of the emitter contact. This also implies that the emitter current $I_{E,}$ equals the sum of base current $I_B$ and the collector $I_C$:

$$I_E = I_C + I_B \qquad \text{..... 5.3.1}$$

The base emitter voltage and base collector voltage is positive if a positive voltage is applied to the base contact relative to emitter and collector respectively.

The operation is illustrated with figure 5.34 (b). We consider here only the forward active bias mode operation, obtained by forward biasing the base-emitter junction and reverse biasing the base collector junction. To simplify we also set $V_{CE} = 0$. The corresponding energy band diagram is shown in figure 5.35.

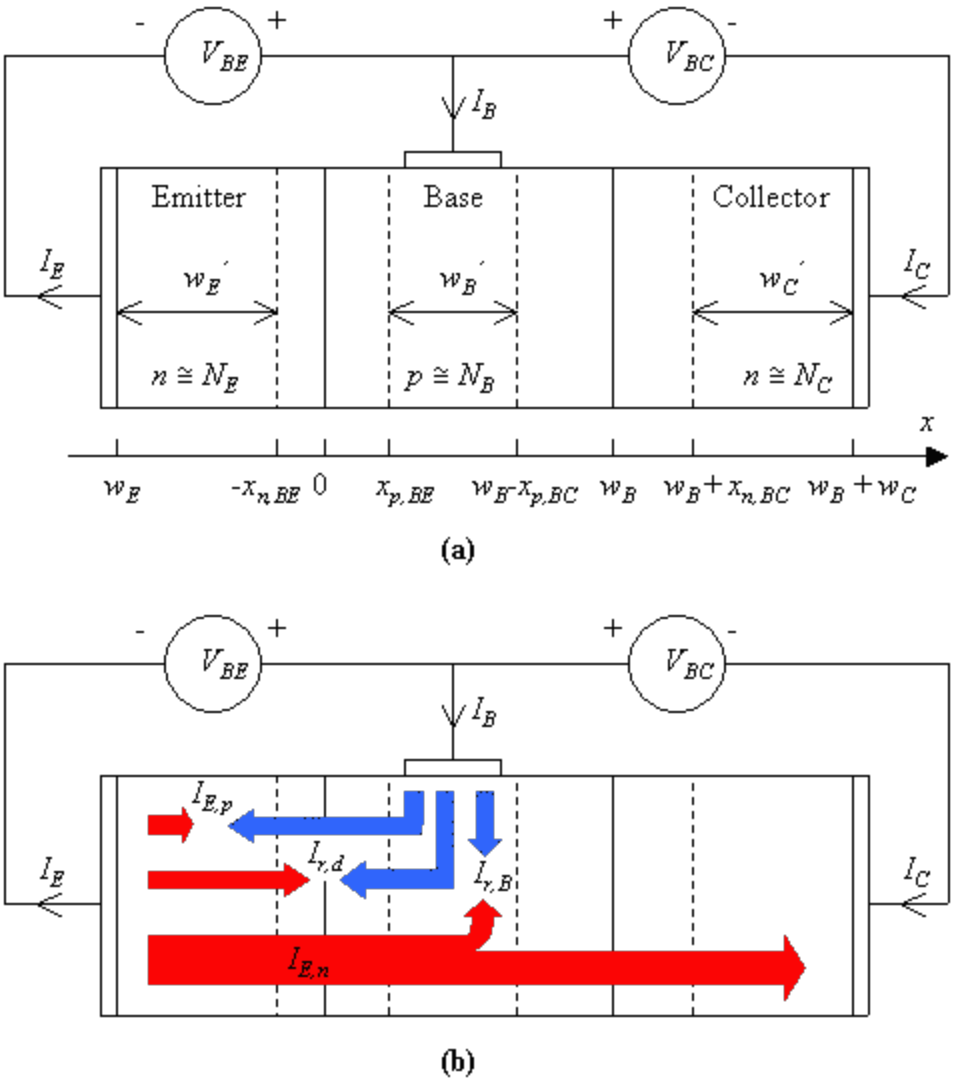



Figure 5.34: (a) Structure and sign convention of a npn bipolar junction transistor

(b) Electron and holes flow under forward active bias, $V_{BE} > 0$ and $V_{BC} = 0$

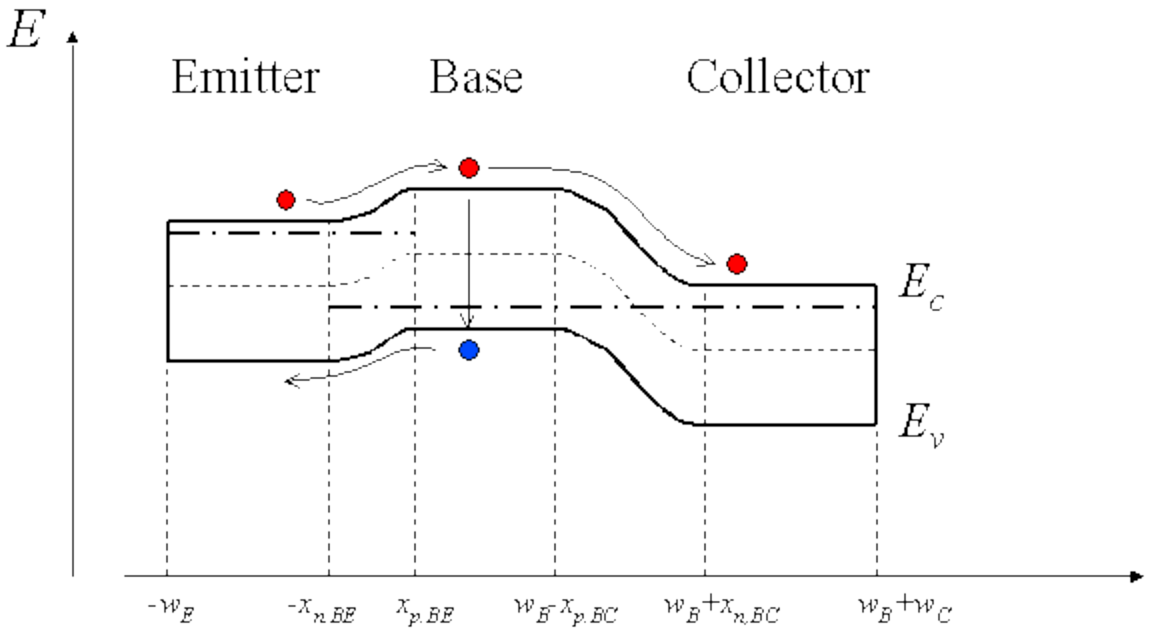



Figure 5.35: Energy band diagram of a bipolar transistor biased in the forward active Region

The total emitter current is the sum of the electron diffusion current $I_{E,\,n}$, the hole diffusion current $I_{E,\,p}$ and the base emitter depletion layer recombination current $I_{r,\,d}$,

$$I_E = I_{E,n} + I_{E,p} + I_{r,d} \qquad \text{..... 5.3.2}$$

The total collector current is the electron diffusion current, $I_{E,\,n}$ minus the base recombination current, $I_{r,\,B}$.

$$I_C = I_{E,n} - I_{r,B} \qquad \text{..... 5.3.3}$$

The base current is the sum of the holes diffusion current, $I_{E,\,P}$ , the base recombination current, $I_{r.\,B}$ , and hence the base emitter current $I_{r,\,d}$ .

$$I_B = I_{E,p} + I_{r,B} + I_{r,d} \qquad \text{..... 5.3.4}$$

The transport factor $\alpha$ is defined as the ration of the collector current and emitter current:

$$\alpha = \frac{I_C}{I_E} \qquad \text{..... 5.3.5}$$

Using Kirchoff's current law and sign convention shown in figure 5.34 (b), we find that the base current equals the difference between the emitter and collector current. The current gain, $\beta$ , is defined as the ratio of the collector and base current and equals:

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha} \qquad \text{…….. 5.3.6}$$

This explains how a bipolar junction transistor can provide current amplification. If the collector current is almost equal to the emitter current, the transport factor, $\alpha$ , approaches one. The current gain, $\beta$ , can therefore become much larger than one.

We now rewrite the transport factor, $\alpha$ , as the product of emitter efficiency, $\gamma_r$ , the base transport factor, $\alpha_T$ , and the depletion layer recombination factor, $\delta_r$ ,

$$\alpha = \alpha_T \, \gamma_E \, \delta_r \qquad \text{…….. 5.3.7}$$

The emitter efficiency, $\gamma_E$ , is defined as the ratio of the electron current in the emitter, $I_{E,\,n}$ , to the sum of the electron and hole current diffusing across the base emitter junction, $I_{E,\,n} + I_{E,\,p}$ .

$$\gamma_E = \frac{I_{E,n}}{I_{E,n} + I_{E,p}} \qquad \text{…….. 5.3.8}$$

The base transport factor, $\alpha_T$ , equals the ratio of the current due to electrons injected in the collector, to the current due to electron injected in the base.

$$\alpha_T = \frac{I_{E,n} - I_{r,B}}{I_{E,n}} \qquad \text{…….. 5.3.9}$$

Recombination in the depletion region of the base emitter junction further reduces the current gain, as it increases the emitter current without increasing the collector current. The depletion layer recombination factor, $\delta_r$, equals the ratio of the current due to electron and hole diffusion across the base emitter junction to the total emitter current:

$$\delta_r = \frac{I_E - I_{r,d}}{I_E} \qquad \text{…….. 5.3.10}$$

## 5. 3. 3 MODES OF TRANSISTOR OPERATION:

Transistor can be operated in any of the three modes as drawn in figure 5.36.

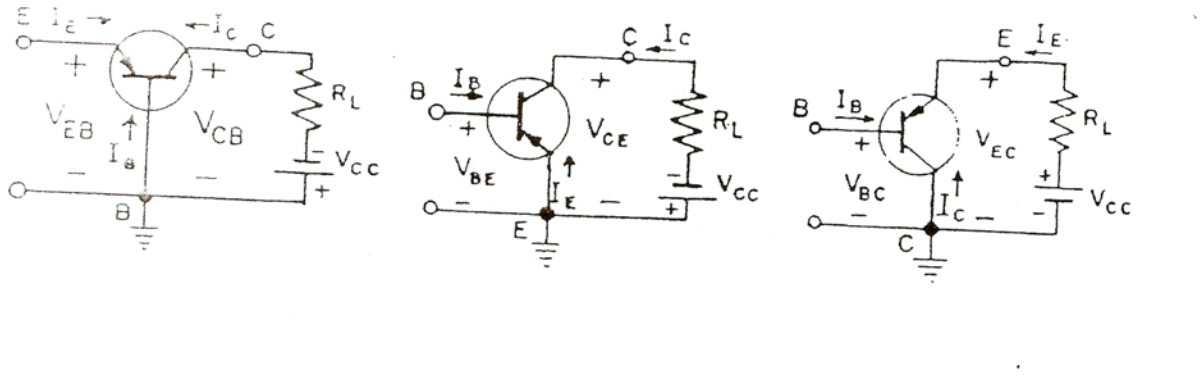



Figure 5.36 Mode of operation of a pnp transistor

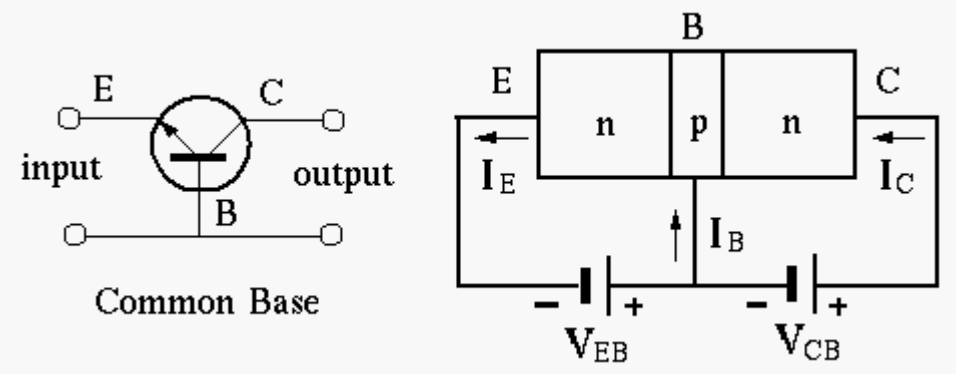
1. Common Base (CB) mode: This configuration is known as the grounded base configuration. The base terminal is common between the input and output circuit. Fig a
2. Common Emitter (CE) Mode: This configuration is known as grounded emitter configuration Emitter terminal is common between input and output circuit. Fig b
3. Common Collector (CC) Mode: When collector terminal is common between input and output circuit, the transistor is sad to operate n grounded collector configuration. Fig c

## 5.3.4 COMMON BASE CONNECTION OR CB CONFIGURATION

Input is connected between emitter and base while output is connected across collector and base.

***<u>Current amplification factor:</u>***

The ratio of output current to input current is known as current amplification factor. In common connection the output current is collector current $I_c$ and input current is emitter current $I_E$.




*Thus ratio of change in collector current to the change in emitter current at constant collector base voltage $V_{CB}$ is known as current amplification factor of a transistor in common base configuration.*

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB}$$

Now $I_E = I_C + I_B$

or $\Delta I_E = \Delta I_C + \Delta I_B$

or $$\frac{\Delta I_E}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_E} + \frac{\Delta I_B}{\Delta I_E}$$

or $$1 = \alpha + \frac{\Delta I_B}{\Delta I_E}$$

or $$\alpha = 1 - \frac{\Delta I_B}{\Delta I_E}$$

This clearly shows that the value of current amplification factor is less than unity. If the value of $I_B$ reduces zero, the value of $\alpha$ approaches unity.

*Practical value of $\alpha$ in commercial transistors varies from 0.95 to 0.99.*

***<u>Collector Current:</u>***

The total collector current consists of:

1. A large percentage of emitter current that reaches the collector terminal i.e. $\alpha I_E$.
2. The leakage current $I_{Leakage}$ . This current is due to the movement of minority carriers across the collector-base junction as the junction is heavily reverse biased.

$\therefore$ The total current $I_C = \alpha I_E + I_{leakage}$

From the expression we note that even if $I_E = 0$, a very small current flows through the collector. This leakage current is known as $I_{CBO}$ i.e. collector base current with emitter circuit open.

$$I_C = \alpha I_E + I_{CBO}$$

## 5.3.5 CHARACTERISTICS OF COMMON BASE CONFIGURATION

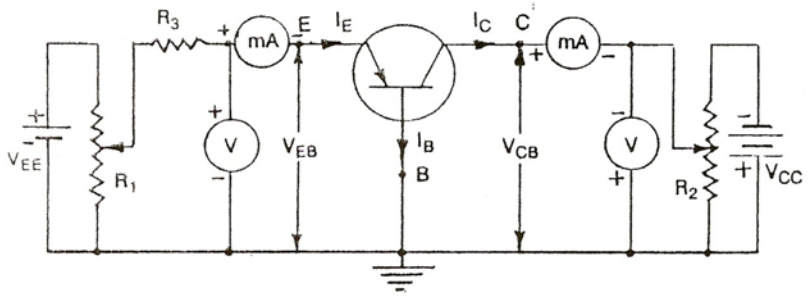



Figure 5.37: The arrangement for common base characteristics of a p-n-p Junction Transistor

***1.Input Characteristics:*** In CB configuration the curve plotted between the emitter current $I_E$ and the emitter base voltage at constant collector voltage is called input characteristics. Figure 5.37 shows the input characteristics of a pnp transistor in CB Configuration.

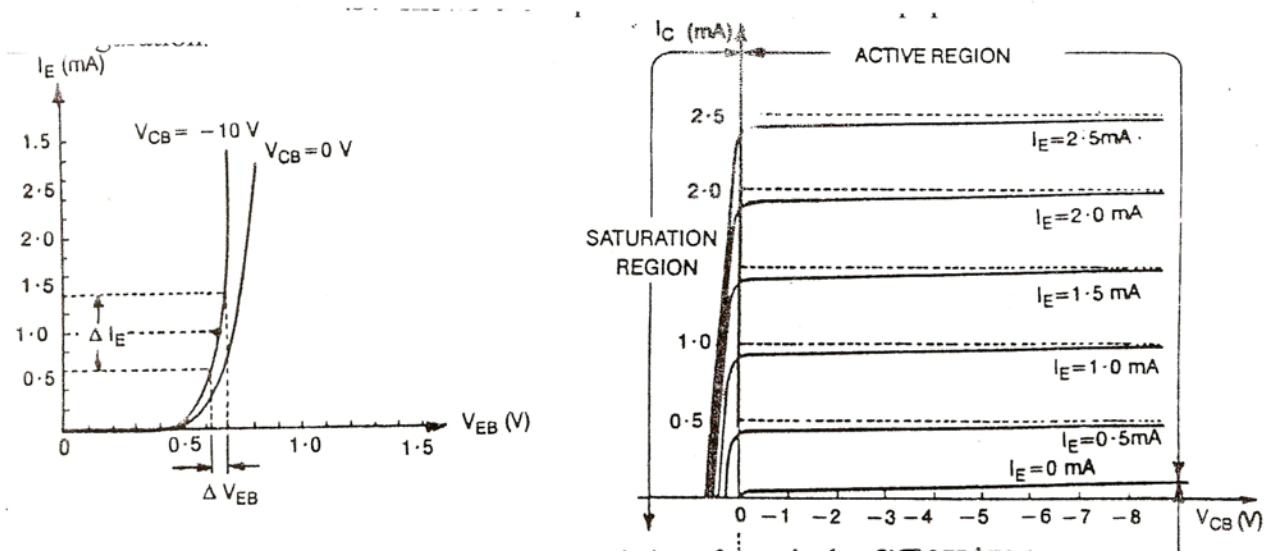



Figure 5.38 (a) Input Characteristics of a typical pnp Transistor
(b) Output Characteristics of a typical pnp Transister

1. For a particular value of $V_{CB}$ the curve is just like a diode characteristics in forward region. P-N emitter junction is forward biased.
2. When $V_{CB}$ is increased, the value $I_E$ increases slightly for a given value of $V_{EB}$. Hence the junction becomes a better diode. It also reveals that emitter current and hence collector current is almost independent of collector base voltage $V_{CB}$.
3. The emitter current $I_E$ increases rapidly with a small increase rapidly with a small increase in emitter base voltage $V_{EB}$. It shows that input resistance is very small.

***Input Resistance:*** *The ratio of change in the emitter base voltage to the resulting change in emitter current at constant collector base voltage is called input resistance.*

Input resistance, $r_i = \frac{\Delta V_{EB}}{\Delta I_E}$ at constant $V_{CB}$

The typical Values of input resistance varies from a few ohms to 100 ohms.

***2. Output Characteristics:*** *In CB configuration the curve plotted between collector current $I_C$ and collector base voltage $V_{CB}$ at constant emitter current $I_E$ is called output characteristic.*

Figure 5.38 (b) shows the output characteristics of a typical pnp Transistor in CB configuration.

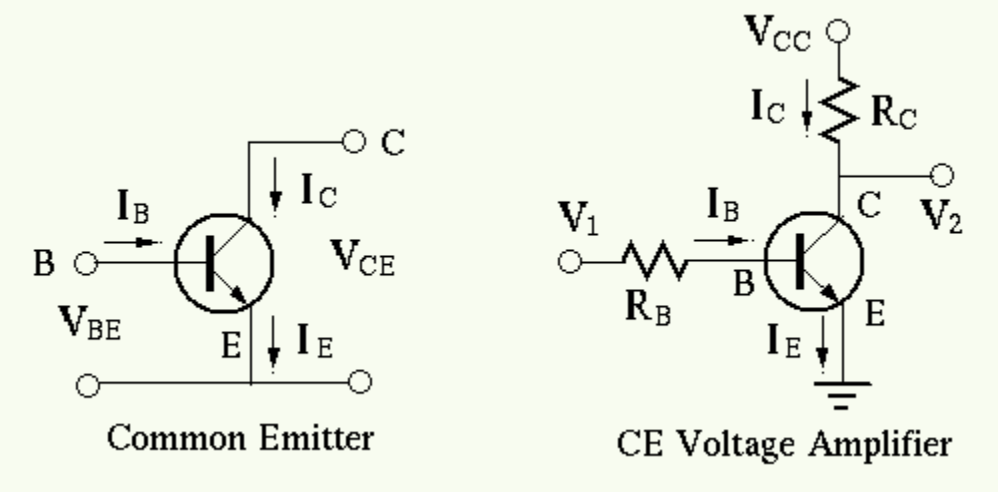
1. In *active region* where collector base junction is reverse biased, the collector current $I_C$ is almost equal to the emitter current $I_E$. The transistor is always operated in this region.
2. In active region the curves are almost flat. A very large change in $V_{CB}$ produces only a tiny change in $I_C$. It means that circuit has very high output resistance $r_0$.
3. When $V_{CB}$ becomes positive i.e. the collector base junction is forward biased, the collector current $I_C$ decreases abruptly. This is a *saturation region*. In this region $I_C$ does not depend upon $I_E$.
4. When $I_E = 0$, collector current $I_C$ is not zero . This is the reverse saturation current $I_{CBO}$ that flows in the collector circuit.

***Output resistance***: *The ratio of change in collector base voltage to the resulting change in collector current at constant emitter current is known as output resistance.*

Output resistance, $r_o = \frac{\Delta V_{CB}}{\Delta I_C}$ at constant $I_E$

Output resistance in CB configuration is very high which is of the order of several tens of kilo ohms ($\cong M\Omega$ ).

## 5.3.6 COMMON EMITTER CONNECTION OR CE CONFIGURATION:



***1. Input Characteristics:***

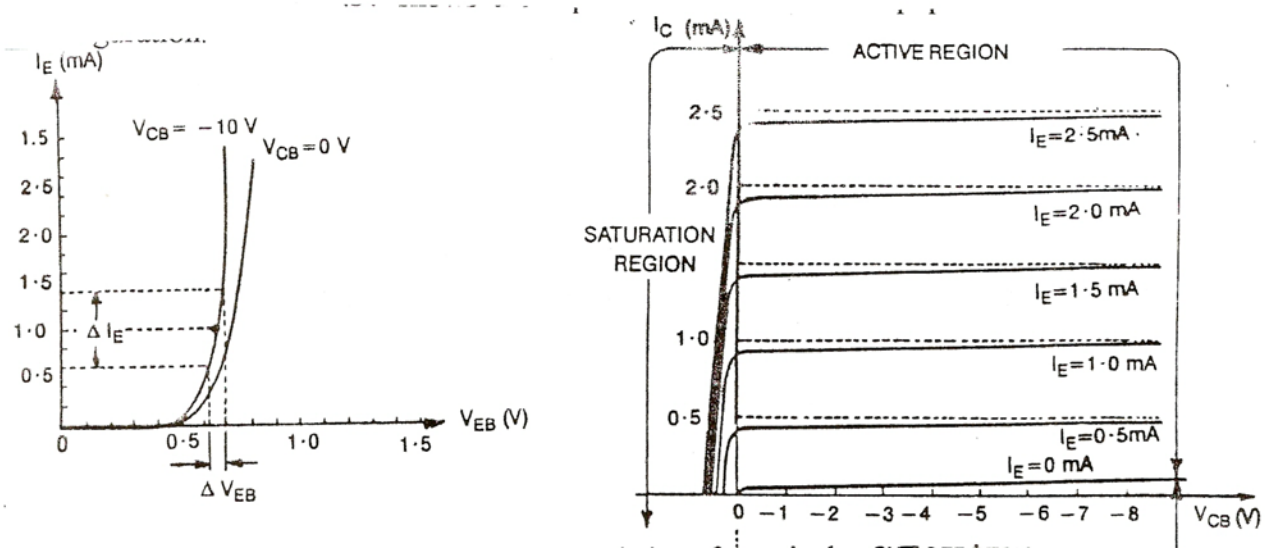



Figure 5.39 (a) Input characteristics of typical npn transistor
(b) Output Characteristics of a typical npn transistor

*In CE configuration the curve plotted between base current $I_B$ and base emitter voltage $V_{BE}$ is called input characteristics.*

1. The curves are similar to those obtained for CB configuration i.e. like a forward diode. The only difference is that $I_B$ increases less rapidly with increase in $V_{BE}$. Hence input resistance is comparatively higher than hat in CB configuration.
2. he change in $V_{CE}$ does not result in a large deviation of curves and hence the effect of change in $V_{CE}$ on input characteristics is ignored for all practical purposes.

***Input resistance:*** The ratio of change in base emitter voltage to resulting change in base current at constant collector emitter voltage is known as input resistance:

Input resistance, $r_i = \dfrac{\Delta V_{BE}}{\Delta I_B}$ at constant $V_{CE}$

The typical values of an input resistance is of the order of few hundred ohms.

***2. Output Characteristics:***

*In CE configuration the curves plotted between collector current $I_C$ and collector emitter voltage $V_{CE}$ at constant base current is called output characteristic.*

1. In active region, $I_C$ increases slightly as $V_{CE}$ increases. The slop of the curve is little bit more than the output characteristics of CB configuration. Hence output resistance $r_o$ of this configuration is less as compared to CB configuration.
2. Since the value of $I_C$ increases with increase in $V_{CE}$ at constant $I_B$ , the value of $\beta$ also increases (as $\beta = I_C/I_B$ ).

3. When $V_{CE}$ falls below the value of $V_{CE}$ (i.e. below few tenths of volts), $I_C$ increases rapidly. In fact at this stage the collector base junction is forward biased and transistor works in the *saturation region*. In saturation region $I_C$ becomes independent of upon $I_B$.
4. In active region $I_C = \beta\ I_B$, and hence a small current $I_C$ is not equal to zero but its value is equal to the reverse leakage current $I_{CEO}$ (i.e. collector to emitter current when base is open).

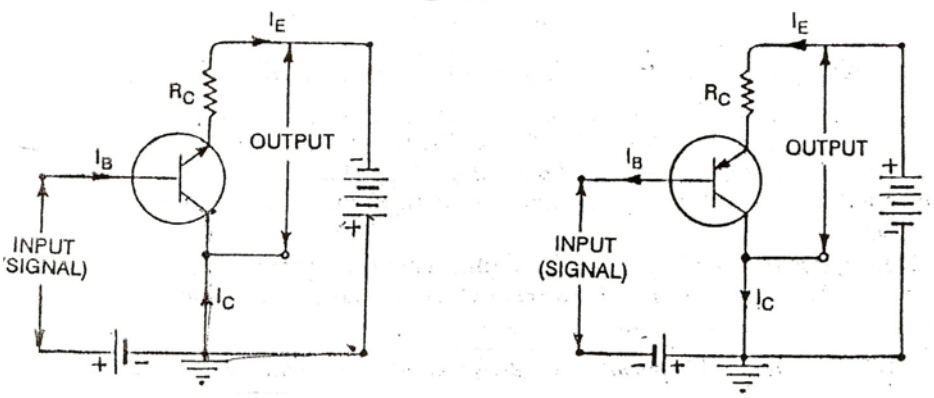
***Output resistance:*** the ratio of change in collector emitter voltage to the change in collector current at constant base current $I_B$ is called output resistance $r_o$.

Output resistance, $r_o = \dfrac{\Delta V_{CE}}{\Delta I_C}$ at constant $I_B$

The typical value of output resistance in CE configuration is of the order of 50 $k\Omega$.

## 5.3.7 COMMON COLLECTOR CONNECTION OR CC CONFIGURATION:

In this case, the output is taken across emitter and as such it is said that the output follows the common emitter, that is why it is called ***emitter follower***.




***Current amplification factor $\gamma$ :***

The ratio of output current to the input current is known as amplification factor. In common collector, the output current is emitter current $I_E$ ,whereas the input current is base current $I_B$.

Thus the ratio of change in emitter current to the change in base current is known as current amplification factor.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

***Relation between $\gamma$ and $\alpha$:***

We know $\gamma = \dfrac{\Delta I_E}{\Delta I_B}$ ……(i)

And $\alpha = \dfrac{\Delta I_C}{\Delta I_E}$ ……(ii)

Now $I_E = I_C + I_B$

or $\Delta I_E = \Delta I_C + \Delta I_B$

or $\Delta I_B = \Delta I_E - \Delta I_C$

Substituting the value of $\Delta I_B$ in equation (i), we get

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C} = \frac{\Delta I_E / \Delta I_E}{\Delta I_E / \Delta I_E - \Delta I_C / \Delta I_E} = \frac{1}{1-\alpha}$$

or $$\gamma = \frac{1}{1-\alpha}$$

The relation above shows that value of $\gamma$ is nearly equal to $\beta$. However arrangement is seldom used for amplification because input resistance is very high and out is very low. So voltage gain is very low.

***Collector current:***

We have seen that $I_C = \alpha I_E + I_{CBO}$

And $I_E = I_C + I_B = (\alpha I_E + I_{CBO}) + I_B$

Or $I_E - \alpha I_E = I_B + I_{CBO}$

Or $$I_E = I_B \frac{1}{1-\alpha} + I_{CBO} \frac{1}{1-\alpha}$$

$$= (\beta + 1) I_B + (\beta + 1) I_{CBO}$$

## 5.3.8 COMPARISON BETWEEN THREE TANSISTOR CONFIGURATIONS:

| No. | Characteristics | Common base configuration | Common-emitter configuration | Common collector configuration |
|---|---|---|---|---|
| **1.** | *Input resistance* | Low (50 ohms) | Low ( 1 KΩ ) | Very High (700 k Ω ) |
| 2. | *Output resistance* | Very high (500 ohms) | High (10 K Ω ) | Low ( 50 Ω ) |
| 3. | *Current gain* | Less than unity | High (100) | High (100) |
| 4. | *Voltage gain* | Small (150) | High ( 500) | Less than one |
| 5. | *Leakage current* | Very small (5 µ A for Ge 1 µ A for Si) | Very Large ( 500 µ A for Ge 20 µ A for Si) | Very large ( 500 µ A for Ge 20 µ A for Si ) |
| 6. | *Application* | For high frequency applications | For Audio frequency applications | For impedance matching |

## 5.3.9 COMMONLY USED TRANSISTOR CONNECTION:

Common Emitter Connections are mostly used out of the three transistor configurations because of following reasons.

1. ***High Current gain***: $I_C$ is the output current and $I_B$ the input current in CE configuration. The value of $I_C$ is much more than input current $I_B$, therefore current gain is very high. It may range from 20 to 500.
2. ***High voltage and power gain***: As the output resistance is nearly 50 times that of input resistance in CE circuits and because of high current gain this type of transistor circuit arrangement ha highest voltage and power gain. This is the major reason for using transistor in this circuit arrangement.
3. ***Moderate output to input impedance ratio***: The ratio of output impedance to input impedance is quite small in Common emitter circuit. *Because of this reason, this circuit arrangement is ideal for coupling between various transistor amplifier stages.*

## 5.3.10 TRANSISTOR AS A SWITCH:

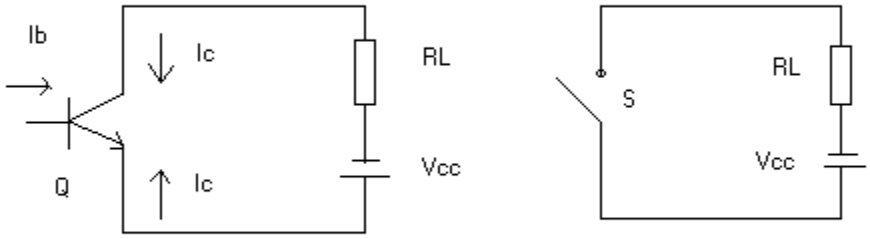



Figure 5.37: Transistor as a switch

Transistor in figure 5.37, is used as a switch to connect or disconnect the load $R_L$ from source $V_{cc}$. Transistor serves the same purpose as that of a mechanical switch shown figure. In the mechanical switch arrangement, no current flows when the switch is open but when the switch is closed all the voltage $V_{cc}$ appears across $R_L$. Transistor also behaves in the similar manner.

It is useful to divide the transistor range of operation into three regions while using it as switch: The *cutoff*, the *active* and the *saturation* region. These regions can be easily identified on the common base characteristics of the transistor as shown in figure 5.36.

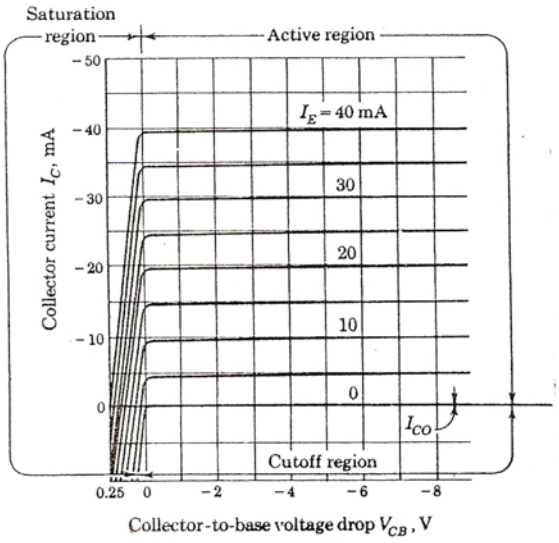



Figure 5.36 Common base characteristics of a pnp transistor

In the cutoff region both emitter and collector are reverse biased and only very small saturation current flow across the junction. The transistor operates in the region below the characteristic for $I_E = 0$. This characteristic corresponds to the collector current $I_{co}$, reverse collector saturation current It is almost coincident with the axis $I_C$. The transistor must be in cutoff region when it is to behave like an open switch.

When the emitter junction is forward biased and the collector junction is reverse biased, the transistor output current responds to the input signal. Transistor switches abruptly from cutoff region to active region.

The region to the left where $V_{CB} = 0$ and above $I_E = 0$ is the saturation region. Here emitter junction and collector junction are both forward biased. The voltage across the individual junction or combination of both junctions is small. Accordingly when transistor switch is required to be in the closed condition it is driven into saturation.

When a transistor is used as a switch in the common base configuration, the input current required to operate the switch is nominally as large as collector current being switched. In common collector configuration, the input voltage required to operate the switch is as large as supply voltage.

In common emitter configuration the input switching signal, current or voltage is small in comparison with switched output current or voltage. Hence the common emitter configuration is most commonly used for transistor switch.

**THE TRANSISTOR AT CUTOFF:**

Cutoff in a transistor is defined by the condition $I_E$ =0. Common base characteristic, to the point of cutoff, is given by the equation

$$I_C = -\alpha I_E + I_{co} \qquad \text{..... 5.40}$$

In which $\alpha$ is the common base short circuit forward current gain. With the cutoff condition $I_E = 0$, we get $I_C = I_{C0.}$

It is important to note that in the common emitter configuration the transistor will not be at cutoff if base is open circuited. In the circuit in figure if $I_B = 0$, then $I_{E} = -I_C$ and from equation 5.40 we have

$$I_C = -I_E = \frac{I_{CO}}{1-\alpha} \qquad \text{..... 5.41}$$

In Germanium even near cutoff, $\alpha$ may be as large as 0.9 and $I_C \approx 10\ I_{CO.}$ Therefore the transistor is not in cutoff. $I_B$ =0 corresponds to a small forward bias and that to bring germanium transistor to cutoff we need to establish a reverse biasing voltage between base and emitter of about 0.1V.

In silicon, at collector of the order of $I_{CO}$, it is found that $\alpha$ is nearly zero because of recombination in the junction transistor region. Hence even with $I_B = 0$ we find from equation 5.41 that $I_C = I_{CO} = -I_{E,}$ so that the transistor is still very close to cutoff. We verify that in silicone, cutoff ($I_{E=0}$) occurs at $V_{BE} \sim 0V$ corresponding to short circuited base.

**The Reverse Collector Saturation Current $I_{CBO}$:**

The collector current when the emitter current is zero is designated by symbol $I_{CBO}$. Two factors cooperate to make $|I_{CBO}|$ larger than $|I_{CO}|$. First there exists a leakage current which flows not through the junction but around it and across the surfaces. The leakage current is proportional to the voltage across the junction. The second reason is why $|I_{CBO}|$ exceeds $|I_{CO}|$ is that new carriers may be generated by collision in the junction transition region, leading to avalanche breakdown. But even before breakdown is approached, this multiplication component of current may attain considerable proportions.

## 5.4 FIELD EFFECT TRANSISTORS:

A field effect transistor (FET) is a three terminal device in which current conduction is by one type carrier (i.e. either electrons or holes) and controlled by the effect of electric field. FET's are of two type:

(a) Junction field effect transistor (JFET)

(b) Metal oxide semiconductors FET (MOSFET).

MOSFET's are further divided into two parts:

(i) depletion enhancement MOSFET i.e. DE MOSFET

(ii) enhancement only MOSFET i.e. E-only MOSFET

## 5.4.1 JUNCTION FIELD EFFECT TRANSISTORS (JFET):

*Construction:*

JFET can be fabricated with either one N-channel or P-Channel though N-Channel is preferred. For fabricating N-Channel JFET, N-type semiconductor material is taken and then two P-type junctions are defused on opposite sides of its middle part as shown in figure 5.37. These junctions form two P-N diodes or gates (G) and area between theses gates is called channels. The two P regions are internally connected and single lead is brought out which is called gate terminal. Ohmic contacts are made at two ends of the N-type semiconductor bars. One terminal is known as source (S) through which the majority carrier (electrons in this case) enter the bar. The other terminal is known as the drain (D) through which these majority carriers leave the bar.

Thus a FET has essentially three terminals i.e. gate (G), source and drain (D).

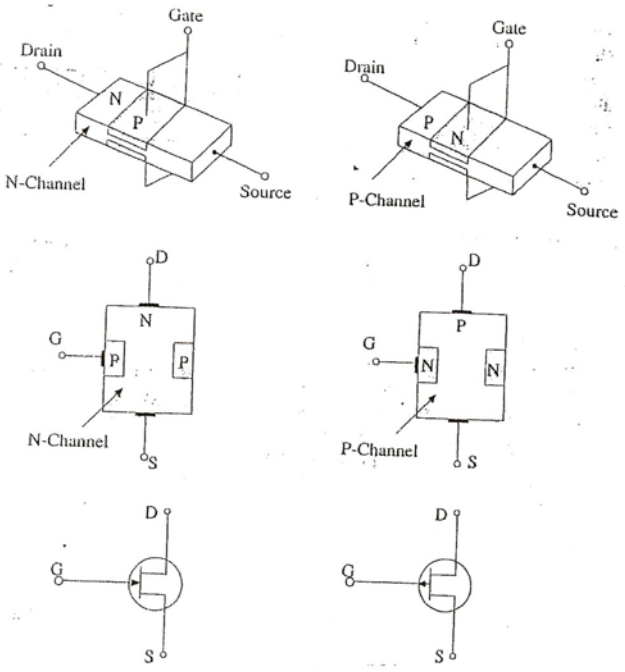



Figure 5.37: Schematic symbols for N-Channel and P-Channel JFET

When potential difference is established between drain and the source, current flows along the length of the bar through the channel located between the two regions. The current consists of only majority carriers which in present case are electrons.
If the bar is of P-type semiconductor and the two islands are of N-type semiconductors, the device is known as P-Channel JFET. The majority carriers in this case are holes which flow through the channel located between the two N-regions or gates. Schematic symbol for N-type channels and P-type channels JFET ate shown in figure. Gate arrow always points to N-type material.

*Operating Principle:*
When a voltage $V_{DS}$ is applied across the drain and source terminals and voltage applied across the gate and source $V_{GS}$ is zero (i.e. the gate circuit is open) as shown in figure 5.38 (a), the two pn junctions establish a very thin depletion layer. Thus a large amount of electrons will flow from source to drain through a wide channel formed between the two depletion layers.

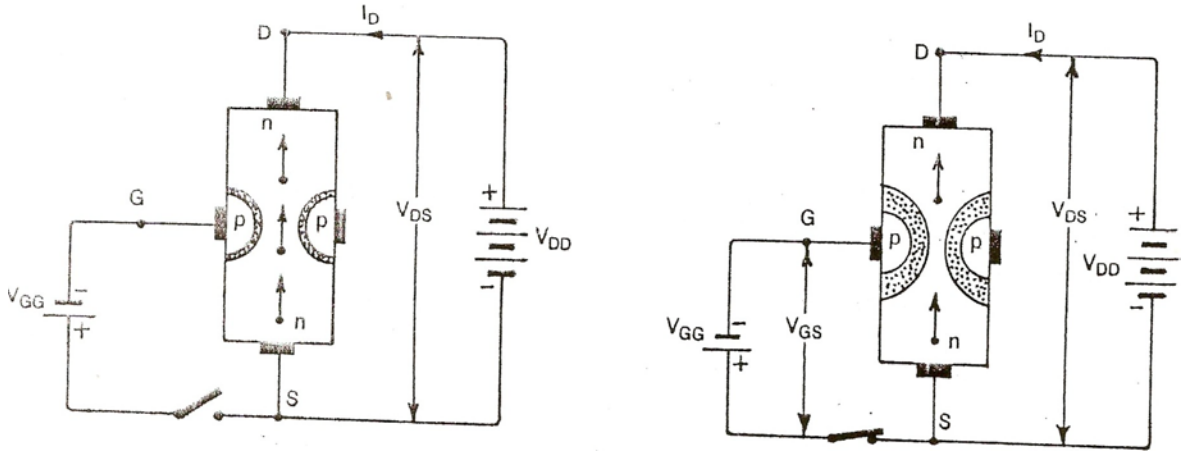



Figure 5.38: Circuit Diagram of an n-channel FET with normal polarities

When a reverse voltage $V_{GS}$ is applied across the gate and source as shown in figure (b), the width if depletion layer is increased. This reduces the width of conducting channel thereby decreasing the conduction (flow of electrons through it. Thus the current flowing from source to drain depends upon the width of the conduction channel which depends upon the thickness of depletion layer. The thickness of depletion layer established by the two junctions depends upon the voltage applied across the gate source terminal.
Hence, it is clear that the current from source to drain can be controlled by the application of potential (i.e. electric field) on the gate. This is why the device is called field effect transistor. P-channel transistors also operates in the same manner as an n-channel FET except that the current carries will be holes instead of electrons and all polarities shall be reversed.

*FET Characteristics:*

A curve drawn between drain current ($I_D$) and drain source voltage of FET at constant gate source voltage is known as output characteristics of the FET.

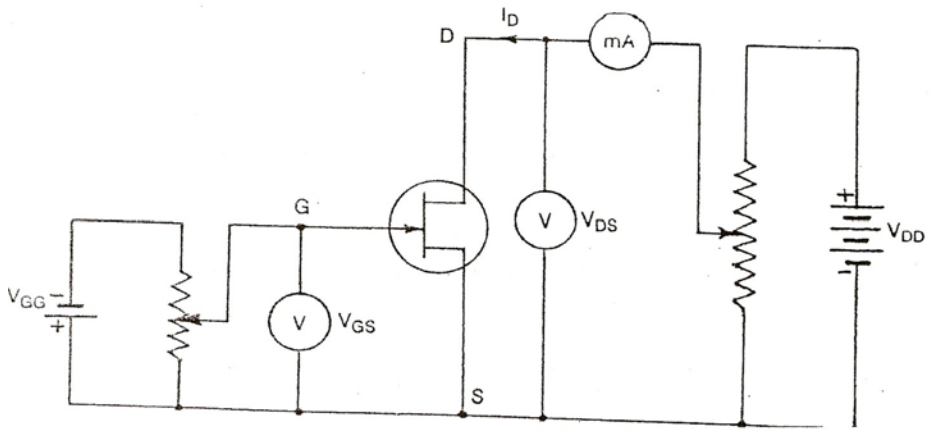



Figure 5.39: Circuit of a FET to determine the characteristics

A circuit as shown in figure is drawn to determine the characteristics of FET. Fix the gate source voltage $V_{GS}$ at some value (say $V_{GS}$ = 0) and from zero increase the drain source voltage $V_{DS}$ in steps. Note the drain current ($I_D$) corresponding to each value of $V_{DS}$ .Plot the curve which shows the output characteristics of a FET. Now after changing the values of $V_{GS}$ to 0,5, 1, 2. 3, 3, 4 volts, repeat the same procedure. Thus we can obtain a family of output characteristics as shown in figure.

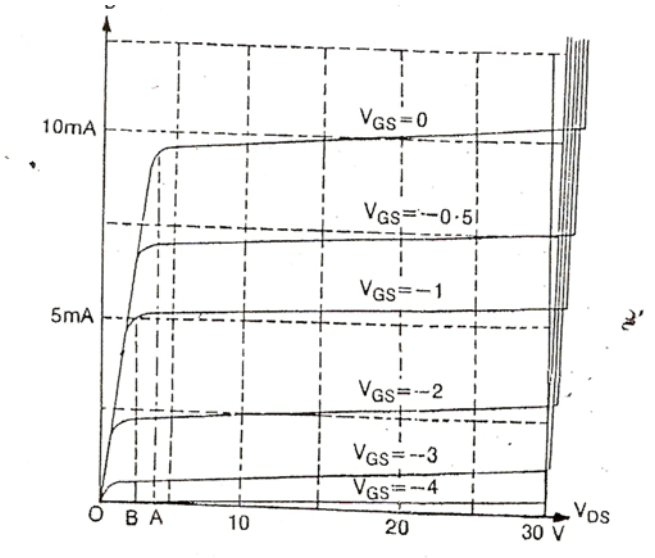



Figure 4.40: Output characteristics of FET

1. At the initial stage, the drain current $I_D$ increases rapidly with increase in drain source voltage $V_{DS}$ but then becomes almost constant.
   *The drain source voltage above which drain current almost becomes constant is known as* ***pinch off voltage.*** OA is pinch off voltage in curve.
2. After pinch off voltage, the depletion layer almost touches each other and conducting channel becomes very narrow. Thereafter the increase in drain current $I_D$ is very small with increase in drain source voltage $V_{DS}$ . Thus drain current almost becomes constant.
3. When the gate source voltage $V_{GS}$ is applied in the direction to provide additional bias, the pinch off voltage will occur at smaller value of pinch off voltage will occur at smaller values of $V_{DS}$ = OB instead of OA.
4. Further increase in drain source voltage $V_{DS}$ eventually cause breakdown across reverse biased gate junction and current $I_D$ shoots to very high value. Since the reverse bias gate voltage adds to drain voltage, the more the reverse bias at the gate, more the effective voltage at the gate junction. Therefore it is seen that in figure 5.41 avalanche occurs at a lower value of $V_{DS}$ .
5. The characteristics just resembles with pentode valve.

## 5.4.2 METAL OXIDE SEMICONDUCTOR FIELD EFFECT TANSISTOR (MOSFET):

Unlike FET the gate is insulated from the channel. The gate current is therefore very small weather the gate is positive or negative.

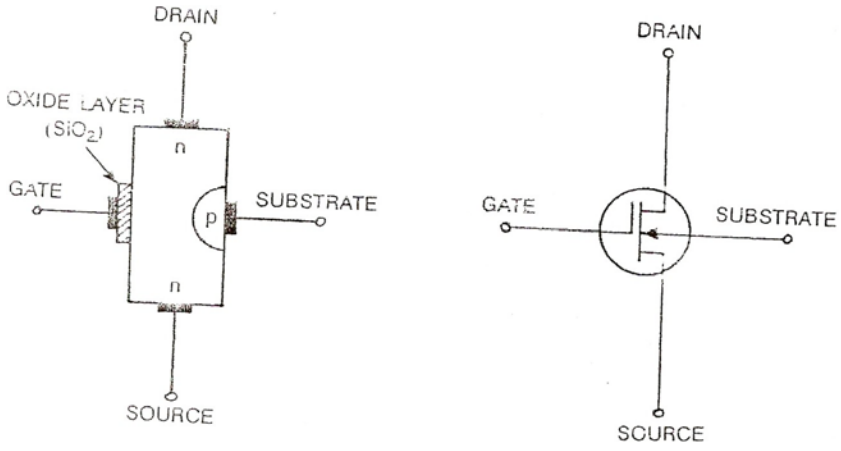



Figure 5.41: View of N-Channel MOSFET

*Construction:*
Figure 5.41 shows the view of N-Channel MOSFET.

1. There is only one p-region instead of two. This region is known as substrate.
2. Over the left side of the channel, this layer of metal oxide ($Sio_2$) is deposited. A metallic gate is deposited over the layer of silicone dioxide. The gate is insulated from the channel since silicone dioxide is insulator. This is why it is called insulated gate FET.
3. Since the gate is insulated from the channel by a thin layer of $Sio_2$, the input impedance of MOSFET is very high.
4. Unlike FET, MOSFET has no gate diode rather it forms a capacitor. The capacitor has gate and channel as electrodes and oxide layer as dielectric. Because of this property the device can be used with negative as well as positive gate voltage.

*Working Principle of MOSFET:*
The circuit diagram of an N-Channel MOSFET with normal polarities is shown in figure 5.42. MOSFET has no gate diode rather it form a capacitor which has two electrodes i.e. gate and channel. When negative voltage is applied to the gate, electrons accumulate on it. The electrons repel the conduction band electrons in N-Channel. Therefore, the number of conduction electrons available for current conduction through the channel will reduce. The greater the negative potential on the gate, the lesser is the current conduction from source drain. However if the gate is given positive voltage, more electrons are made available in the N-Channel. Consequently, current from source to drain increases.

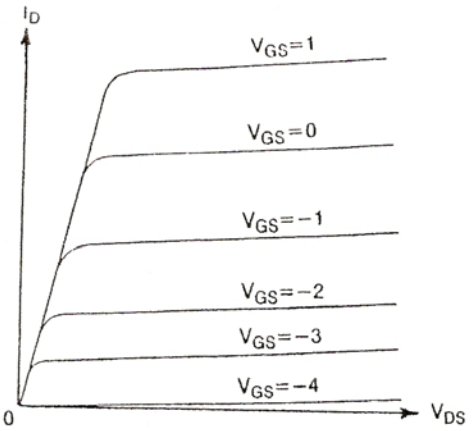



Figure 5.42 Characteristics of a MOSFET

1. In MOSFET, the source to drain current is controlled by electric field setup by the capacitor formed at the gate instead of depletion layer of junction.
2. Unlike the FET, a MOSFET has no gate diode, This is why the device can be operated on negative and positive gate voltage.
3. Since the gate is insulated from the channel by an oxide layer, a negligible gate current flows due to gate capacitance whether the voltage applied at the gate is negative or positive. Consequently, the input impedance, of MOSFET is very high ranging from $10^{10}$ ohms to $10^{15}$ ohms.

## 5.5 INEGERATED CIRCUITS:

The circuit, in which various active and passive components like transistors, diodes, capacitors, resistors etc are integral part of a small piece of semiconductor chip, are called *Integrated Circuits.*
An integrated circuit comprises of various components and their interconnections.
It is possible to produce circuits containing many components, on a very small piece of semiconductor wafer called chip.
The size of chip has dimensions 2mmX2mmX0.1mm.
Since all components are integral part of the chip, no component can be removed or replaced.
No component is projected above the surface of the chip since they are formed within the chip.
The size being extremely small, we need a microscope to see various components and interconnections.

### 5.5.1 CLASSIFICATIONS OF IC's:

*(A)According to their Construction:*

i.) Monolithic IC's: All components are formed as part of single p-type wafer. These IC's are most commonly used in practice.
ii.) Thin film IC's: All components in this type of IC's are formed on ceramic or glass substrate. Evaporation process is used to fabricate such IC's.
iii.) Thick film IC's: In this type of IC's, resistors and capacitors are formed on substrate but transistors are added as discrete components.
iv.) Thin film units are combined on a single substrate but transistors are added as discrete.

*(B) According to their function:*

1. Digital IC's: These are basically pulse circuits and process digital signal.

    (a) VLSI Chip: (Avery Large Scale Integration)
    Chips contain more than 1000 logic gates or integrated components.
    (b) LSI Chips: (Large Scale Integration)
    Chips contain 100 to 1000 logic gates or integrated components.
    (c) MSI Chips: (Medium Scale Integration)
    Chips contain 10 to 100 logic gates or integrated components.
    (d) SSI Chips: ( Small Scale Integration )
    Chips contain less than 12 logic gates or integrated components.

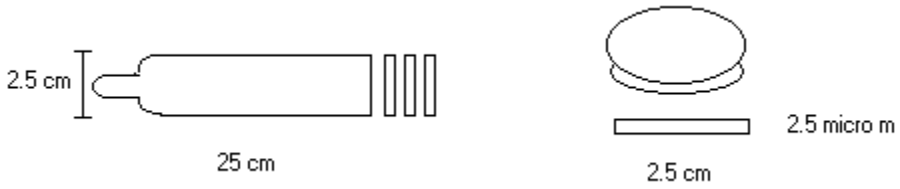
2. Linear IC's:

These IC's process analog signals. Analog signals are that signal which varies continuously in proportions to its input. Linear IC's contain small amplifiers circuits for either audio or RF signals.

## 5.5.2 A MONOLITHIC IC'S:

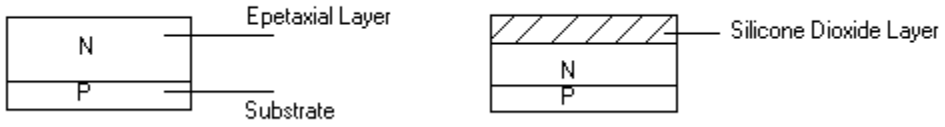
Monolithic means 'single' and Litho means 'stone'. Thus Monolithic means single stone or one stone.
All components are fabricated on the same wafer (single).

***P-Substrate:***




We first prepare a wafer of p-type semiconductor. A cylindrical crystal is grown having typical dimensions 5cm long and 2.5 cm diameter. The crystal is then cut by diamond saw into many slices called wafers of 200 $\mu$m thickness. We call this p-type wafer as substrate on which transistors and other components are built.

*Ep**etaxial n-layer:***
An n-type epetaxial layer typically 20 $\mu$m thick is grown onto the p-type substrate as shown in diagram.




For growing epetaxial layer, the wafer are put in a diffusion furnace and a gas mixture of silicon atoms and pentavalant impurity atoms is passed over the wafer which forms a thin layer of n-type semiconductor on the heated surface of substrate. All the active and passive components are fabricated within this layer using number of diffusion steps.

*Insulating layer:*
A thin layer about 1 $\mu$m of silicon dioxide $Sio_2$ is deposited over the entire surface of the epetaxial layer as shown in figure This is achieved by passing pure oxygen over epetaxial layer which when combines with silicone atoms form a layer of $Sio_2$. This thin glass

insulating layer protects the silicon surface against contamination. This also acts as barrier in the selective diffusion process in epetaxial layer.

*Etching:*
In the selected regions when diffusion is to take place. Silicone dioxide layer is removed and a window is provided leaving rest of the wafer protected against diffusion. The process of removal is called etching and is achieved by photochemical techniques.

*Producing Components:*
After etching the $Sio_2$ layer, by diffusion various components like diodes, transistors, resistors and capacitors are formed on the wafer.

*Metallic Path:*
Metallic paths are needed to interconnect various fabricated components of IC chip. These are essentially alluminium printed wires. These paths are terminated at the edge of the chip where they are bonded with thin for connections to the external leads or IC pins.

## 5.6 PULSE TRANSFORMERS:

## 5.6.1 PULSE TRANSFORMERS APPLICATIONS:

Iron cored transformers are used in the transmission and shaping of pulses with width range of nanoseconds to about 25 $\mu$ sec. Applications of pulse transformers are:

1. To change the amplitude and impedance level of a pulse.
2. To invert the polarity of a pulse. Also a center taped winding provides equal positive and negative pulses simultaneously.
3. To produce a pulse in a circuit having negligible dc resistance.
4. To provide a dc isolation between a source and a load
5. To couple between stages of pulse amplifiers
6. To differentiate a pulse
7. To act as a coupling element in certain pulse generating circuits.

## 5.6.2 TRANSFORMER MODELS:

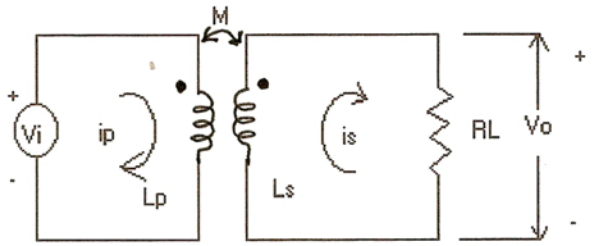



Figure 5.41: Schematic diagram of a transformer including load and source

The schematic diagram of a transformer is indicated in the figure 5.41. Primary inductance is $L_p$, the secondary inductance is $L_S$, and the mutual inductance is M. The load resistance is $R_{L.}$ To begin with le us ignore primary, secondary, and source resistance and all capacitances. Also ignore core loses and nonlinearity of magnetic circuit.

The coefficient of coupling K between primary and secondary is defined by

$$K = \frac{M}{L_P L_S}$$

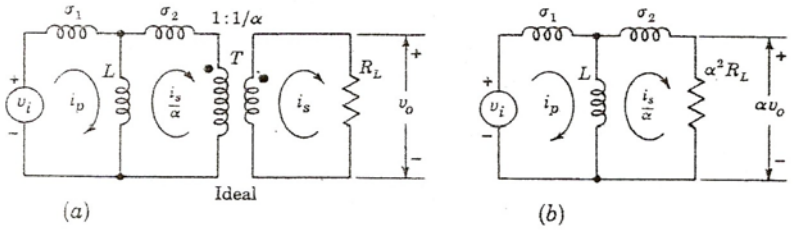
Under the circumstances mentioned above the ideal transformer is one by which $L_P$ is infinite and K = 1 in this case the output $V_0$ is an exact replica of the input $V_i$ and transformer ratio n is independent of load.

For the ideal transformer:

$$\frac{V_0}{V_i} = \frac{i_p}{i_S} = \sqrt{\frac{L_s}{L_p}} = \frac{N_s}{N_p} = n \qquad \text{……..5.50}$$

where, $i_p$ is primary current, $i_s$ is secondary current, $N_p$ is the primary number of turns and $N_s$ is secondary number of turns.

*A pulse transformer behaves as a perfect transformer when used in connection with the fast waveform it is intended to handle*. In such a case it is advantageous to replace the actual transformer by an ideal transformer together with additional circuit components.




(a) (b)

Figure 5.42 : (a) A circuit which is equivalent to that of figure 5.41. In which an ideal transformer T having a voltage step-up ratio $1/\alpha$ is introduced.
(b)The same circuit with transformer T eliminated by reflecting the secondary load into the primary

Circuit in figure 5.42a and 5.42 b are two equivalent circuits of figure 5.41. The figure 5.41 includes an ideal transformer cascaded with a configuration of inductor. The transformer ratio of the ideal transformer T is $1/\alpha$ = secondary voltage/primary voltage, where $\alpha$ is a number. The load current has been reflected into the primary as $i_s/\alpha$. The ideal load resistance $R_L$ has also been reflected into primary side in figure 5.42b as a resistance $\alpha^2 R_L$. We shall now find out the values of parameters $\sigma_1, \sigma_2$, and L in terms of $\alpha$, $L_P$ , $L_S$ and M.

The circuit of figure 5.42b is to be equivalent to the original transformer in circuit in the sense that both are to draw the same current $i_P$ from the source $V_i$ and both are to furnish the same current $i_s$ to the load $R_L$.

In the circuit of figure 5.41 we may write the mesh equations

$$V_i = L_P \frac{di_P}{dt} - M\frac{di_S}{dt} \qquad \text{..... 5.51a}$$

$$0 = -M\frac{di_P}{dt} + L_S\frac{di_2}{dt} + i_S R_L \qquad \text{..... .....5.51b}$$

The corresponding equation for circuit of figure 5.42b are

$$Vi = (\sigma_1 + L)\frac{di_P}{dt} - L\frac{d}{dt}\left(\frac{i_2}{\alpha}\right) \qquad \text{.....5.51a}$$

$$0 = -L\frac{di_P}{dt} + (\sigma_2 + L)\frac{d}{dt}\left(\frac{i_S}{\alpha}\right) + \alpha^2 R_L\left(\frac{i_S}{\alpha}\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots 5.51b$$

Dividing the equation 5.51b by $\alpha$ and then if equations 5.50 and 5.51are compared, we find them to be identical provided that

$$L_P = \sigma_1 + L \qquad M = \frac{L}{\alpha} \qquad L_S = \frac{\sigma_2 + L}{\alpha^2} \qquad \ldots\ldots\ldots 5.52$$

or

$$L = \alpha M \qquad \sigma_1 = L_P - \alpha M \qquad \sigma_2 = \alpha^2 L_S - \alpha M \quad \ldots\ldots\ldots 5.53$$

We are at liberty to select $\alpha$. The circuit which results, together with corresponding values, are shown in figure 5.43 a, b, c, for choices

$\alpha = \sqrt{L_P / L_S}$ , $\alpha = (1/K)\sqrt{L_P L_S}$ or $\alpha = K\sqrt{L_P L_S}$

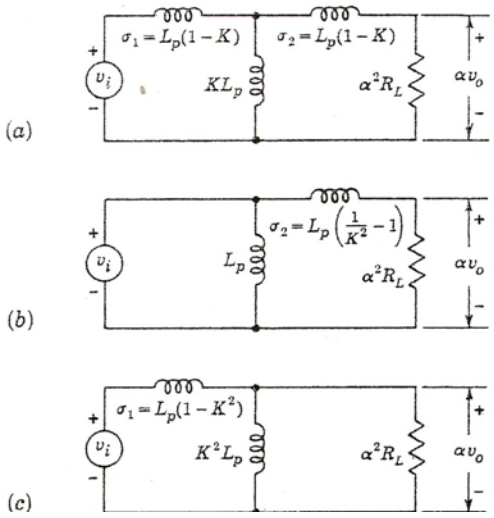



Figure 5.43 The forms of the circuit of figure 5.42b for three particular values of $\alpha$

The results shown are calculated directly from the equation 5.43 combined with definition of coupling

$$K = M/\sqrt{L_P L_S}$$

In the figure 5.43a $\sigma_1 = \sigma_2$ in figure 5.43b $\sigma_1 = 0$ and in figure 5.43c $\sigma_2 = 0$

In a well constructed pulse transformer the coefficient of coupling K differs from unity by 1%. Hence

$1 - K^2 = (1-K)(1+K) \sim 2(1-K)$

And for such transformer (K~1), each of the circuit of figure 5.43 gives nearly the same value for the total series inductance and total shunt inductance. The total series inductance called leakage inductance, equals t or has value

$$\sigma \sim 2L_P(1-K) \qquad \ldots\ldots\ldots\ldots\ldots 5.54$$

and shunt resistance has a value equals to

$$L \approx L_P \qquad \text{.....5.55}$$

We also have

$$\frac{1}{\alpha} \approx n \qquad \text{.....5.56}$$

Model of figure 5.43 c is most useful model for studying transmission of pulses through a transformer.

## 5.6.3 COMPLETE EQUIVALENT CIRCUIT:

Consider a simple case of a single layer of $N_P$ turns wound in a solenoid form and the secondary consists of a single layer wound concentrically with it. The secondary has $N_S$ turns. Let us assume the sizes of both windings are different but length is same. Let us consider that transformer is connected between the source and the load as shown in figure 5.44.

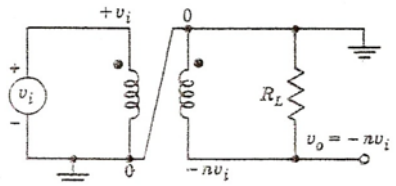



Figure 5.44: An inverting transformer with turns ratio n

We have connected the opposite ends of the winding to common ground. Assuming that the windings are wound in the same direction on the core, the transformer must invert the input.

$$V_0 = -(N_S/N_P)\, V_i = -n\, Vi$$

Now there is a voltage nV between the bottom end of the windings. Voltage decreases linearly with distance along the winding and equals $V_i$ at the top. There exists an electric field between the space of the two winding and in this space electrostatic energy is stored.. The circuit element which stores energy is called Capacitance. Therefore we have to add to the Model of transformer in figure 5.43C, a capacitance C. The addition is made in the circuit given in figure 5.45.

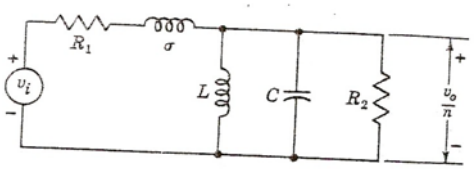



Figure 5.45: The equivalent circuit of a transformer, including resistance and total shut capacitance C

We have taken the transformer capacitance into account by including a shunt capacitance C which is connected on the load side of leakage inductance. Since the capacitance is a distributive element and no matter which location is selected. Let us describe the reason of locating this capacitance at the load end. If C were located on the input side and the input has a zero input impedance, the effect of this capacitance would disappear. Secondly, the external shunt loading capacitance $C_L$ encountered with a pulse transformer is very frequently heavier on the output side and this capacitance reflected with primary side may simply be added to the transformer capacitance. In figure 5.45 we have included as well resistance $R_1$ which represents the sum of primary winding resistance and generator impedance. The resistance $R_L$ represents the combination of load resistance $R_L$ and secondary winding resistance $R`_L$ so that

$$R_L = \frac{R_L + R_2'}{n^2}$$

## 5.6.4 TRANSFORMER INDUCTANCE;

From the circuit 5.43 it is clear that the magnetic inductance is the inductance presented at the input terminals when the secondary is open circuited. Or more simply the magnetic induction is the primary winding inductance .similarly the leakage inductance is the inductance presented at the terminals of primary when the secondary is short circuited.

The primary inductance $L_P$ may be calculated from a simple magnetic circuit given in figure 5.46.

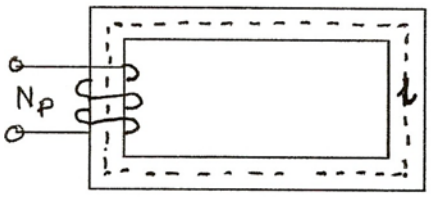



Figure 5.46 A primary of $N_P$ turns is wound on a magnetic core of mean magnetic path length l

If l is the mean length of magnetic path, A the cross section area of the core, $N_P$ the number of primary turns and $\mu$ the magnetic permeability,

$$L_P = \frac{\mu A N_P}{l} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.57$$

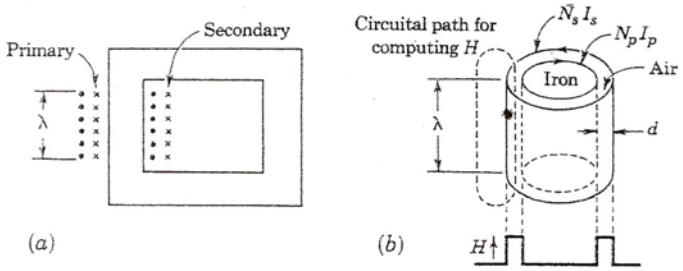



Figure 5.47: (a) A one layer secondary wound directly over a one layer primary.
(b) A schematic view of the windings considered as current sheets, and magnetic flux between windings

Consider a simple geometrical arrangement given in figure 5.47. When a single layer is wound over a one layer primary, we already noted that secondary must be short circuited in order to find $\sigma$. For this connection the output voltage is zero. Hence the net flux in the iron core is zero and the primary and secondary ampere turns must be equal and oppositely directed $N_P I_P = N_S I_S$. The whole flux appears in the space between the coils. Almost all flux appears in the space between the coils. For simplicity we replace the coils by current sheets carrying currents $N_P I_P$ and $N_S I_S$ respectively. A drawing of concentric solenoidal windings is shown in figure 5.47 and the magnetic field intensity H between winding is also indicated. The current sheets are same length $\lambda$ as the coil is long. The value of H in the region between sheets is

$$H = N_P I_P / \lambda$$

The energy density stored in the magnetic field is given by

$$\frac{1}{2} \mu H^2$$

Accordingly the total energy W is

$W = \frac{1}{2} \mu_0 H^2 V$, where V is the volume between coils and when we have replaced by $\mu$ by $\mu_0$ the permeability of free space medium which is air.

The energy may also be calculated from

$W = \frac{1}{2}\sigma I_P^2$ since the magnetic energy resides in the leakage inductance $\sigma$

Equation the two equation we get

$$\sigma = \frac{\mu_0 H^2 V}{I_P^2} = \frac{\mu_0 N_P^2 V}{\lambda^2} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.58$$

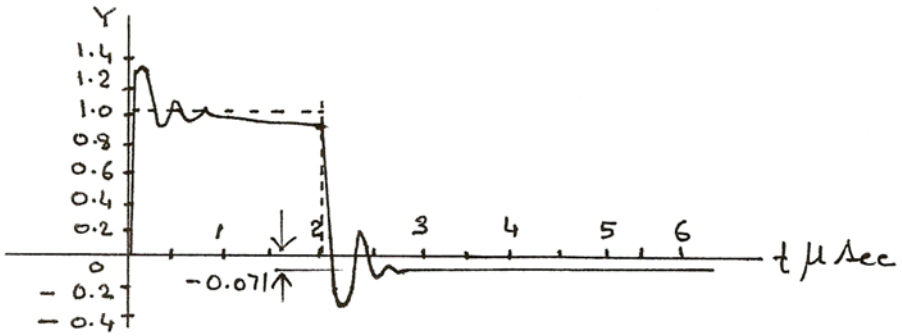
where all quantities are expressed in mks. This calculation indicates that $\sigma$ is due to the leakage flux that is the flux which links one but both windings.

Second method of determining the $\sigma$ is to short the secondary, shunt the primary with capacitance $C_1$, and measure the resonant frequency $f_1$. In order to eliminate the effect of the unknown capacitances which are in shunt with $C_1$, the above measurement is repeated with second capacitor $C_2$

$$\sigma = \frac{f_1^2 - f_2^2}{(2\pi f_1 f_2)^2 (C_2 - C_1)} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 5.59$$

## 5.6.5 PULSE TRANSFORMERS GENERAL CONSIDERATIONS:

An ideal transformer, which would introduce none of the pulse distortions, would have a infinite L and zero $\sigma$ and C.




Actually the magnetizing inductance determines the tilt during the pulse and backswing at the end of the pulse. To determine tilt and backing we require $L >> R\ t_P$

For the required magnetizing inductance we have to select a suitable core in both material and geometry and then calculate the turns on the primary side. The number of secondary turns are determined from the transformer ratio.

Preservation of pulse shape is important in small pulse transformers. The winding resistance will therefore have to have very large resistance. It is often 10% more than

load resistance. Small wires are therefore used to reduce capacitance. Inter winding space t be kept small, so that leakage inductance is kept small.
The finite rise time and ringing observed in the transformer response results I from the leakage inductance $\sigma$ and capacitance C. Since the number of turns on the winding is fixed by required by the required magnetic inductance, all we may do in connection with $\sigma$ and the capacitance C is to decrease one at the expense of increasing other. The is in principal at leas one remedy that both minimize $\sigma$ and C and increase $L_P$ arbitrarily. This method consists of employing a core material whose magnetic permeability is infinite. For such a case, a one turn primary would provide more than adequate magnetizing inductance. And since the turns are minimal we may shrink the spacing between "winding" so that $\sigma$ vanishes without introducing a capacitance.
In order to reduce eddy current, to minimize both losses and skin effect, it is important that the core be laminated.

## 5.6.6FERRITE TRANSFORMERS:

Cores molded from a magnetic ceramic such as sintered manganese-zinc ferrite are excellent for pulse transformers. The permeability is not very great, but resistivity is at least 10 million times that of Permalloy. This high resistivity means that skin effect due to eddy currents is very small and effective permeability of the order of 1,000 is attained.. Also loss is very small and Q of the order 5 to 15 is obtained at a frequency of 1 M Hz. One form of this ferrite core is shown in figure 5.48.
The winding are placed on a circular nylone or paper bobbin, which is then inserted in the core. An end view of the complete core, assembled by putting two cores together, is indicated in figure.5.48.

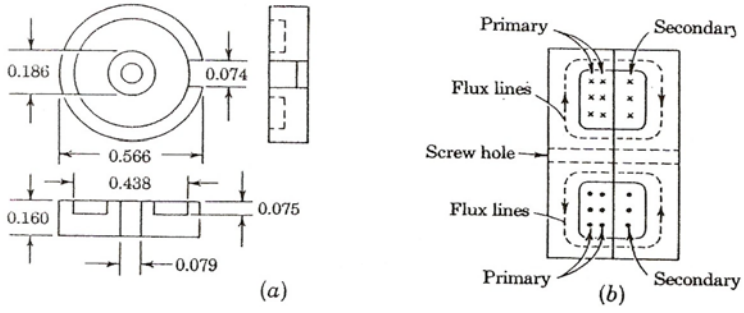



Figure 5.48: (a) Three views of a small ferrite pot core (b) The assembled transformer

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# CAMAC Model 2551 12-Channel 100 MHz Scaler

* Compact packaging-12 channels per single-width module means fewer crates, smaller systems, less inhibit fan-out.
* Low cost-The high density hybrid circuit design allow common functions to serve a greater number of channels, thus lowering the cost per channel.
* Fast clear Input-Enables fast rejection of unwanted data without dataway operations.
* Less than 10 ns double-pulse resolution-1 00 MHz counting rates.
* Direct-coupled Inputs-Input sensitivity or rate capability are not dependent upon risetime.
* Input Inhibit-Common inhibit disables inputs without injecting counts.
* Test mode-Increment mode permits testing all scalers simultaneously without removing cables.
* Full LAM functions-Signals impending overflow condition.
* Full provision to cascade channels-provides > 24-bit capacity when needed.

The LRS Model 2551 contains 12 identical 24-bit binary scalers especially designed for use in high- speed nuclear counting applications. This dramatic increase in channel density over conventional 4-channel designs is made possible by state-of-the art hybrid circuits which offer reliability-enhancing low power dissipation in addition to compact packaging.

Each scaler is equipped with an extremely wideband input circuit which responds to NIM level logic signals of any duration down to 5 ns, without multiple-pulsing (in the case of wide inputs) and without counting down. The ability to recognize narrow input signals at an equivalent rate of >100 MHz is an important feature, since it assures that the scaler will accurately accumulate any output signal gener- ated by standard discriminator and logic circuits.

Each module is provided with a high-speed fast inhibit which permits simultaneous rejection of input signals at a rate equivalent to 100 MHz. The CAMAC Inhibit (1) provides inhibit control via the rear connector.The inhibit signal must overlap the input signal, but toggling the inhibit will not cause pulses to be counted.

Fast rejection of unwanted data is provided by the fast clear input. This input allows the entire scaler to be reset by application of a NIM level clear pulse without the need to perform any dataway operations.

The Model 2551 provides a full set of LAM functions. When enabled, setting of the 24th bit of any of the 12 channels is flagged by generation of LAM.

The Model 2551 has a built-in test circuit which allows all registers to be checked simultaneously. Application of the CAMAC Increment F(25) Function Code causes each

scaler to advance by one count for each S2 timing signal received. The test circuit may be used without disconnecting cables if the Input or CAMAC I Inhibit is on. The 24-bit data from any scaler is read in parallel to the common dataway via the rear card-edge connector. Individual channel non-destructive readout is accomp- lished by generating a CAMAC Read F(O) and the appropriate address. Using Read and Clear F(2), the channels will be automatically zeroed after reading the last channel. Clear F(9), CAMAC Clear C, or Initialize Z will zero all channels.

The LRS Model 2551 12-Channel 100 MHz Scaler embodies refinements developed over years of experience width wideband direct-coupled discrimination and counting circuits, and, as a result, offers flexibility, reliability, and performance unmatched by any other available equipment.

**SPECIFICATIONS CAMAC Model 2551 12-CHANNEL 100 MHz SCALER**

| | |
|---|---|
| Signal Input (each channel): | Threshold: > -600 mV (NIM logic levels). |
| Impedance: | 50Ohm, direct-coupled. |
| Reflection: | < 10% typical at 1 ns risetime. |
| Protection: | +/-5 volt transients. |
| Minimum PulseWidth: | 7 ns FWHM at -600 mV input amplitude; 5 ns FWHM at > -700 mV input amplitude. |
| Multiple-Pulse Resolution: | 10 ns. |
| Counting Rate: | DC to 100 MHz. |
| Signal Inhibit: | Common input, -500 mV threshold, 5 ns minimum width, impedance 50 Ohm. Inhibit signal stretches internally by approx. 5 ns and must precede input signal by 10 ns. Inhibit pulses will not be counter by scaler. |
| Half Scale Flag: | Any scaler generates LAM when 24th bit is set. |
| Front-Panel Clear: | Common input, -500 mV threshold, 50 ns minimum width clears all channels with 1 us. |
| Capacity: | 24 binary bits (1 6,777,216), (or 48 bits by cascading channels). |
| Cascading of Channels: | By internal wire jumper option, each even-numbered channel (i.e., 0, 2, 4, 6, 8, 1 0) may be cascaded with the subsequent odd-numbered channel to provide one 48-bit scaler. In this mode of operation, no LAM will be generated by either of the cascaded channels. |
| **CAMAC Commands:** | |
| C: | All scalers and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. |
| Z: | Same as C, except also disables LAM. |
| 1: | All Scaler inputs are inhibited during CAMAC "Inhibit" command. |
| Q: | A Q = 1 response is generated in recognition of an F(O) or F(2) Read function, or an F(8) if LAM set set for a valid N and A, but there will |

| | |
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| | be no response (Q=O) under any other condition. |
| X: | An X=l (Command Accepted) response is generated when a valid F, N, and A command is generated. |
| L: | A Look-At-Me signal is generated from time when first 24th bit is set until a module Clear command. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. |
| **CAMAC Function Codes:** | |
| F(O): | Read registers; requires N and A, A(O) through A(l 1) are used for channel addresses. |
| F(2): | Read registers and Clear module and LAM; requires N and A; (Clears on A(l 1) only.) |
| F(8): | Test Look-At-Me; requires N, and any A from A(O) to A(l 1) independent of LAM disable; Q response is generated if LAM is set. |
| (F(9): | Clear All scaler channels simultaneously; requires N, S2, and A from A(O) to A(l 1). |
| F(24): | Disable Look-At- Me; requires N, S2, and any A from A(O) to A(l 1). |
| F(25): | Increment all scalers; requires N, S2, and any A from A(O) to A(l 1). (inhibit should be true to prevent input pulses from being counted). |
| F(26): | Enable Look-At- Me; requires N, S2, and any A from A(O) to A(l 1). Remains enabled until Z or F(24). |
| CAUTION: The state of the LAM mark will be arbitrary after power turn-on. | |
| Packaging: | In conformance with CAMAC standard for nuclear modules (ESONE Committee Report EUR4100e). RF shielded CAMAC #1 module. |
| Current Requirements: | +6 V at 1.2 A<br>-6 V at 100 mA |

## CAMAC Model 2228A Octal Time-to-Digital Converter

The LeCroy Model 2228A is an Octal Time-To-Digital Converter, packaged in a No. 1 CAMAC module. It incorporates all the advanced operating characteristics which experience has indicated necessary for accurate and reliable measurement of nanosecond time intervals. The Model 2228A has 8 independent channels, each of which measures the time from the leading edge of a common start pulse to the leading edge of its individual stop pulse. Each 2228A channel disregards any stop pulses received before a start signal and will accept only one stop for every start. Conversion begins upon receipt of the start signal, and proceeds until one of the following: a stop signal is received; the cycle is terminated by the application of a front-panel clear signal; or the TDC reaches full scale.

The 2228A converts the measured time intervals into a 11-bit digital number at the rate of 20 MHz, for a full scale digitizing time of 100 mSec. Rear panel control of full-scale and conversion slope permits digitization to fewer bits and a shorter conversion time if desired. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuarcy introduced by the free- running oscillators in conventional designs. LAM, if enabled, is generated at the end of the conversion interval.

The 2228A has three switch-selectable full-scale time ranges, 100, 200 and 500 nSec, which are digitized to 95% of 11 bits (2048 channels) and provide 50, 100, and 250 pSec resolutions respectively. Longer time ranges (up to 10 uSec) may be provided on request at slight expense of stability and accuracy. On line testing is

facilitated by either a front panel common stop input of F(25). A signal at the common stop input generates simultaneous stops for each channel, permitting accurate testing of both front end and scaler section of the module and uniform system testing and time calibration. F(25) is provided for a quick test of the front end and scaler sections with a time measurement of 80% of full scale. In higher rate or colliding beam experiments, excessive system deadtime due to false starts. may be eliminated through use of the 2228A's fast clear input. Accepting NIM level signals, this input allows the TDC to be cleared at any point in its conversion cycle without the necessity for any Dataway operations. All standard LAM functions are available in the 2228A to facilitate data readout. To minimize readout time, both Q and LAM may be suppressed if the module does not contain data.

### SPECIFICATIONS CAMAC Model 2228A OCTAL TIME-TO-DIGITAL CONVERTER

| | |
|---|---|
| Stop Inputs: | 8, one per channel, 50 Ohm impedance; Lemo-type connectors; direct-coupled; input amplitude > -450 mV; ineffective unless preceded by a "Start" input. |
| Common Start Input: | One, common to all channels, 50 Ohm impedance; Lemo-type connector; input amplitude > -450 mV. |

| | |
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| Common Stop Input: | One, common to all channels, 50 Ohm impedance; Lemo-type connector;> -450 mV; functions identical to individual "Stop Inputs" above; used for on-line testing. |
| Fast Clear | One input, common to all channels; Lemo-type connector; 50 Ohm impedance; -450 mV or greater clears; minimum duration 50 nSec. Requires 1.4 uSec after start of clear signal to settle to 1 +/- 1 counts. (However, if the unit is always cleared at a fixed time before each start, it will settle to a constant offset with a small uncertainty, effectively permitting fast reset times on the order of 500 nSec.) |
| Full-Scale Time Range: | 11-bit binary output corresponds to 100, 200, and 500 nSec nominal, switch-selectable (with longest range field-adjustable up to 1 usec). Larger full-scales possible by factory option up to 10 uSec. Both the full-scale value and conversion slope are rear-panel adjustable, permitting faster conversion at the expense of range. |
| Integral Non-linearity: | +/- 2 counts (20 nSec to full scale). |
| Differential Non-linearity: | Channel widths vary by +/-10% (10 nSec to full scale). |
| Time Resolution: | 50 pSec on 100 nSec range; 100 pSec on 200 nSec range; 250 pSec on 500 nSec range. |
| Temperature Coefficient: | Typically (+/-0.02% of full scale +/-0.01% of reading) per degree C. |
| Digitizing Time: | CAMAC modes conversion is initiated by receipt of "Start" input. Approximately 100 uSec for 11 bits; rear- panel adjustable for fewer bits, shorter conversion time. |
| Readout Time: | Readout may proceed at the fastest rate permitted by the CAMAC standard after digitizing is complete. |
| Test Functions: | An internal start/stop is generated by F(25) with approximately 80% of full scale spacing. On-line testing and calibrations can be done with common start and common stop above. |
| Data: | The proper CAMAC function and address command gates the binary data of the selected channel onto the R(1) to R(11) (2^0 to 2^10) Dataway bus lines. The full-scale number of bits, and thus the conversion time, can be selected by a rear-panel pot and test point. (Conversion curve provided with unit.) The overflow flag is always presented on R(12). |
| **CAMAC Commands:** | |
| Z or C: | All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2". |
| I: | "Start" input is inhibited during CAMAC "inhibit" command. |
| Q: | A Q=1 response is generated in recognition of an FO or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but |

| | |
|---|---|
| | there will be no response (Q=0) under any other condition. The Q response for empty modules is suppressed (see 0 and LAM suppression). |
| X: | An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated. |
| L: | Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enable or Disable function command, and can be tested by Test LAM. Switch-selectable option causes LAM to be suppressed by empty modules. |
| **CAMAC Function Codes:** | |
| F(0): | Read registers; requires N and A. A(0) through A(7) are used for channel address. |
| F(2): | Read registers and clear module; requires N, A, and S2. Clears on A(7) only. |
| F(8): | Test Look-At-Me; requires LAM, N and any A from A(0) to A(7). Q is Generated if LAM is present and enabled. |
| F(9): | Clear module (and LAM); requires N and any A from A(0) to A(7), and S2. |
| F(10): | Clear Look-At-Me; requires N, S2 and any A from A(0) to A(7). |
| F(24): | Disable Look-At-Me; requires N, S2 and any A from A(0) to A(7). |
| F(25): | Test module; requires N, S2 and any A from A(0) to A(7). |
| F(26): | Enable Look-At-Me; requires N, S2 and any A from A(0) to A(7). Remains enabled until Z or F(24) applied. |
| Caution: The state of the LAM mask will be arbitrary after power turn-on. | |
| Q and LAM Suppression: | A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches. |
| Packaging: | In conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583.) RF-shielded CAMAC #1 module. |
| Power Requirements: | +24V at 25 mA;<br>-24V at 140 mA;<br>+6V at 600 mA;<br>-6V at 550 mA. |

## CAMAC Model 2249A 12 Channel A-to-D Converter

The LRS Model 2249A 12-Channel Analog-to-Digital Converter embodies all the operational characteristics which have proved important for general-purpose use in high energy particle physics, including expanded resolution (0.1%), higher sensitivity, excellent stability, faster digitizing rate, LAM and Q suppression, provision for fast clear, calibrating test mode, and flexible LAM options.

These ADCs are specifically intended for use in demanding applications such as particle identification using de/dx counters, recording x-ray, neutron, or recoil proton energies using lead glass or other total energy absorbtion counters, improving time resolution by correcting for slewing due to var- iances in counter output amplitudes, monitoring gas threshold Cerenkov counters, and debugging or monitoring proportional or drift chambers.

The Model 2249A contains twelve complete ADC's in a single-width CAMAC module. Each ADC offers a resolution of ten bits to provide 0.1% resolution over a wide 1024-channel dynamic range. The factor of 4 wider range allows operations with broad signal spectra such as are encountered in experi- ments anticipating fractionally charged particles or covering extensive energy ranges. It also greatly reduces the necessity for careful adjustment of signal strengths to match the limited range of an 8-bit, 256-channel instru- ment. The input sensitivity of the Model 2249A is 0.25 pC/count for a full- scale range of 256 pc. This is compatible with most available signal sources and no additional buffering or reshaping of any kind is required to digitize nanosecond pulses.

The excellent long-term stability, temperature characteristics, and isolation between ADC channels assure accurate and reliable performance under the demanding conditions encountered in actual experiments. Confirmation of operation and calibration is provided by the unique test feature which allows all twelve ADC's or an entire system to simultaneously digitize a charge proportional to a dc level provided to a front-panel Lemo connector or patched into Pi, P2 or P5 of the Dataway connector.

The Model 2249A offers excellent event rate capability through the incorpo- ration of a fast clear and a fast digitizing rate. The fast clear input enables the ADC to begin digitizing on the command of a prompt gate and be reset, if necessary, before the end of conversion on the basis of delayed logic or chamber information.This feature eliminates the long input delay cables now required in these situations.

End of conversion of modules which contain data is flagged by generation of a CAMAC LAM. Readout of modules which do not contain information can be eliminated either by use of the LAM signals or through Q suppression.

## SPECIFICATIONS Model 2249A 12 CHANNEL ADC

| | |
|---|---|
| Analog Inputs: | Twelve; Lemo-type connectors; charge-sensitive (current-integrating); direct-coupled, quiescently at approximately +4 mV; 50 Ohm impedance; linear range normally -2 mV to - 1 V; protected to +/- 50 volts against 1 usec transients. |
| Full-Scale Range: | 256 pC +/- 5%. |
| Full-Scale Uniformity: | +/- 5%. |
| Integral Non-linearity: | +/-.25% of reading +/- 0.5 pC (12 pC to 256 pC) for > 500 Ohm source. |
| ADC Resolution: | 10 bits actual, (0.1%). |
| Long-Term Stability: | Better than 0.25% of reading +/- 0.5 pC/week (at constant temperature). |
| Temperature Coefficient: | Typical, 0; max., +/- [.03% of reading (in pC) + .002t] pC/'C (where t = gate duration in nanoseconds, with 50 Ohm reverse termination). |
| ADC Isolation: | A 5-volt, 20 ns overload pulse in any one ADC disturbs data in any other ADC by no more than 0.25 pC. |
| Gate Input: | One gate common to all ADC'S; LEMO-type connectors; 50 Ohm impedance; - 600 mV or greater enables; minimum duration, 1 0 ns; maximum recommended duration, 200 ns (actual limit approximately 2 microseconds with reduced accuracy; partial analog input must occur within 0.5usec after opening gate to preserve accuracy), effective opening and closing times: 2 ns; internal delay, 2 ns. |
| Fast Clear: | One front-panel input common to all ADC'S; LEMO-type connector; 50 Ohm impedance; -600 mV or greater clears, minimum duration, 50 ns. (Caution: narrower pulses cause partial clearing.) Requires additional 2.0 As settling time after clear. |
| Residual Pedestal: | Typically 1 + 0.03t picocoulombs (where t = gate duration in nanoseconds) with 50 Ohm reverse termination. |
| Test Function: | With CAMAC I present, the positive DC level applied to front panel "Test" input (internal high impedance connection to + 12 volts) or optional rear connector P1, P2, or P5 patch points will inject charge with a proportionality constant of - 12.5 pC/volt into all inputs at F(25) . S2 time. (With CAMAC I not present, F(25) - S2 will generate the ~80 ns gate only, providing a measure of residual pedestal only.) |
| Digitizing Time: | 60 us. By factory option, 8-bit operation at 12.5 us digitizing time may be provided. |
| Readout Time: | Readout may proceed at the fastest rate permitted by the CAMAC standard after digitization is complete. |
| Readout | Ready for readout when LAM signal appears. Refer to ESONE |

| | |
|---|---|
| Control: | Committee Report EUR4100e and EUR4600e for additional timing details, voltages, logic levels, impedances, and other standards. |
| Data: | The proper CAMAC function and address command normally gates the 1 0 binary bits plus overflow bit of the selected channel onto the R1 to R1 1 (20 to 210) Dataway bus lines. |
| **CAMAC Commands:** | |
| Z or C: | ADC's and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM. |
| 1: | Gate input is inhibited during CAMAC "Inhibit" command. (Test Function is enabled.) |
| 0: | A Q = 1 response is generated in recognition of an F(0) or F(2) Read function or an F(8) function if LAM is set for a valid "N" and "A", but there will be no response (Q =0) under any other condition. The Q response for empty modules can be suppressed. (See Q and LAM suppression.) |
| X: | An X = 1 (Command Accepted) response is generated when a valid F, N, and A command is generated. |
| L: | A Look-At-Me signal is generated from end of conversion until a module Clear or Clear LAM. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command, and can be tested by Test LAM. Standard option causes LAM to be suppressed for empty modules. |
| **CAMAC Function Codes:** | |
| F(0): | Read registers; requires N and A, A(0) through A(1 1) are used for channel addresses. |
| F(2): | Read registers and Clear module and LAM; requires N and A; (Clears on A(1 1) only.) |
| F(8): | Test Look-At-Me; requires N and any A from A(0) to A(l 1) independent of Disable Look-At-Me. Q response is generated it LAM is set. |
| F(9): | Clear module and LAM; requires N, S2, and any A from A(0) to A(11). |
| F(10): | Clear Look-At-Me; requires N, S2, and any A from A(0) to A(11). |
| F(24): | Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11). |
| F(25): | Test module; requires N, S2, and any A from A(0) to A(11). |
| F(26): | Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24) applied. |
| Caution: The state of the LAM mask will be arbitrary after power turn-on. | |
| Q and LAM Suppression: | Adjustable potentiometer (accessed from side of module) sets count level required (from 0 to 100) before data is considered usefull. A |

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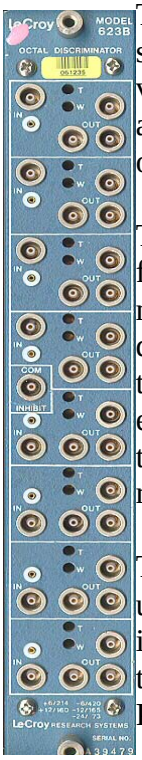
|---|---|
| | module in which all channels contain less than set amount will produce no Q-response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The LAM suppress portion can be disabled with a solder jumper option. |

## NIM Model 623B Octal Updating Discriminator With Inhibit




The Model 623B is a low cost eight channel discriminator featuring high-sensitivity, high-speed, updating performance. A Common Inhibit adds to the versatility of the Model 623B which may be used as an enable for pulsed-mode applications. This discriminator, based upon the proven popular Model 623, offers high density eco- nomically.

The minimum threshold of the Model 623B is -30 mV, variable up to -1 V via front- panel screwdriver adjustment. A monitor point is provided to permit measurement of the threshold level with a voltmeter rather than the more difficult and less precise analog measurement via oscilloscope. The stability of the threshold is <0.2%/'C, assuring accurate results even in varied operating environments. Because of the extremely low reflections from its input (4%), the 623B is significantly better protected against the multiple-pulsing due to reflections at -30 mV.

The Model 623B operates at maximum rates in excess of 100 MHz. Its updating design permits retriggering even while an output from a previous input is still present. At minimum output width setting the 623B will respond to a second pulse within 9 nsec of the leading edge of the first pulse. Propagation delay through the 623B is approximately 11 nsec.

The outputs of the 623B are low impedance voltage outputs, providing output levels greater than -800 mV into a 50 Ohm load. The output durations may be independently set via front-panel screwdriver adjustment from <6 nsec to >150 nsec. Output risetimes are typically 2.1 nsec. Output falltimes increase with output width from approximately 4 nsec at short widths to approximately 7% of the output width at maximum.

```
   SPECIFICATIONS
    NIM Model 623B
 OCTAL UPDATING DISCRIMINATOR WITH INHIBIT

 SIGNAL INPUT CHARACTERISTICS

 Individual Signal:
 Threshold:  -30 mV to approximately -1.0 volt; front-panel screwdriver
adjust (screw-
   driver included).

 Impedance:  50 Ohm +/- 1%, protected to +/-5A for 0.5 Asec clamping at
+1 and -7 volts.

 Reflections:  <4% for input pulses of 2 nsec risetime.

 Stability:  <0.2%/'C, 20'C to 60'C operating range.

 Offset:  0 +/- 1 mv.

 Threshold Monitor:  10:1 ratio of monitor voltage to actual voltage.
```

Common Inhibit:
Input: Accepts NIM standard inputs. -600 mV disables all channels.

Impedance: 50 Ohm +/- 5%.

Timing: NIM pulse must precede analog input by 6 nsec to inhibit. Minimum width 8
nsec. Effective width 5 nsec less than NIM input width.

OUTPUT CHARACTERISICS

Amplitude: 3 NIM-level voltage outputs, quiescently 0 volts, -800 mV during output.

Duration: <=6nsec to >150 nsec, continuously variable via front-panel screwdriver
control.

Risetime: Typically 2.1 nsec; maximum 2.5 nsec. At least 2 outputs should be termi-
nated in 50 fl for optimum pulse shape.

Falltime: Approx. 4 nsec at minimum width, increasing with width setting up to 10 nsec
max.

Width Stability: Maximum +/- (50 psec + 0.3%)/'C for temperature variation and +/-0.1%/% for
variation of any supply voltage.

Amplitude Stability: Better than +/-0.1%/'C.

GENERAL

Maximum Rate: >100 MHz, input and output.

Double-Pulse Resolution: Less than 9 nsec.

Time Slewing: 1 nsec for input amplitudes 110% of threshold and above.

Input-Output Delay: 1 1 nsec.

Multiple-Pulsing: None; one and only one output pulse of preset duration is produced for
each input pulse, regardless of input pulse amplitude or duration.

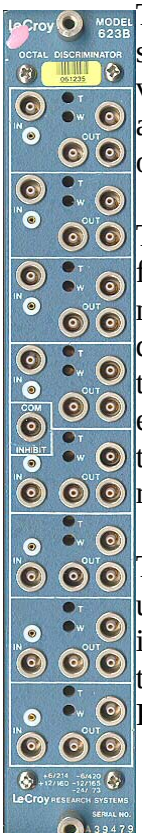
Bin Gate: Slow gate via rear connector and rear-panel ON-OFF switch; risetimes and
falltimes approximately 50 nsec; clamp to ground from +5 volts inhibits;
direct-coupled.

Packaging: In RF-shielded AEC/NIM #1 module; Lemo-type connectors.

Current Requirements:  + 12 volts at 160 mA
  + 6 volts at 240 mA
  - 6 volts at 490 mA
  - 1 2 volts at 195 mA
  -24 volts at 80 mA

---

## NIM Model 623B Octal Updating Discriminator With Inhibit




The Model 623B is a low cost eight channel discriminator featuring high-sensitivity, high-speed, updating performance. A Common Inhibit adds to the versatility of the Model 623B which may be used as an enable for pulsed-mode applications. This discriminator, based upon the proven popular Model 623, offers high density eco- nomically.

The minimum threshold of the Model 623B is -30 mV, variable up to -1 V via front- panel screwdriver adjustment. A monitor point is provided to permit measurement of the threshold level with a voltmeter rather than the more difficult and less precise analog measurement via oscilloscope. The stability of the threshold is <0.2%/'C, assuring accurate results even in varied operating environments. Because of the extremely low reflections from its input (4%), the 623B is significantly better protected against the multiple-pulsing due to reflections at -30 mV.

The Model 623B operates at maximum rates in excess of 100 MHz. Its updating design permits retriggering even while an output from a previous input is still present. At minimum output width setting the 623B will respond to a second pulse within 9 nsec of the leading edge of the first pulse. Propagation delay through the 623B is approximately 11 nsec.

The outputs of the 623B are low impedance voltage outputs, providing output levels greater than -800 mV into a 50 Ohm load. The output durations may be independently set via front-panel screwdriver adjustment from <6 nsec to >150 nsec. Output risetimes are typically 2.1 nsec. Output falltimes increase with output width from approximately 4 nsec at short widths to approximately 7% of the output width at maximum.

```
   SPECIFICATIONS
    NIM Model 623B
 OCTAL UPDATING DISCRIMINATOR WITH INHIBIT

 SIGNAL INPUT CHARACTERISTICS

 Individual Signal:
 Threshold:  -30 mV to approximately -1.0 volt; front-panel screwdriver
adjust (screw-
   driver included).

 Impedance:  50 Ohm +/- 1%, protected to +/-5A for 0.5 Asec clamping at
+1 and -7 volts.

 Reflections:  <4% for input pulses of 2 nsec risetime.

 Stability:  <0.2%/'C, 20'C to 60'C operating range.

 Offset:  0 +/- 1 mv.
```

Threshold Monitor: 10:1 ratio of monitor voltage to actual voltage.

Common Inhibit:
Input: Accepts NIM standard inputs. -600 mV disables all channels.

Impedance: 50 Ohm +/- 5%.

Timing: NIM pulse must precede analog input by 6 nsec to inhibit. Minimum width 8
nsec. Effective width 5 nsec less than NIM input width.

OUTPUT CHARACTERISICS

Amplitude: 3 NIM-level voltage outputs, quiescently 0 volts, -800 mV during output.

Duration: <=6nsec to >150 nsec, continuously variable via front-panel screwdriver
control.

Risetime: Typically 2.1 nsec; maximum 2.5 nsec. At least 2 outputs should be termi-
nated in 50 fl for optimum pulse shape.

Falltime: Approx. 4 nsec at minimum width, increasing with width setting up to 10 nsec
max.

Width Stability: Maximum +/- (50 psec + 0.3%)/'C for temperature variation and +/-0.1%/% for
variation of any supply voltage.

Amplitude Stability: Better than +/-0.1%/'C.

GENERAL

Maximum Rate: >100 MHz, input and output.

Double-Pulse Resolution: Less than 9 nsec.

Time Slewing: 1 nsec for input amplitudes 110% of threshold and above.

Input-Output Delay: 1 1 nsec.

Multiple-Pulsing: None; one and only one output pulse of preset duration is produced for
each input pulse, regardless of input pulse amplitude or duration.

Bin Gate: Slow gate via rear connector and rear-panel ON-OFF switch; risetimes and
falltimes approximately 50 nsec; clamp to ground from +5 volts inhibits;
direct-coupled.

```
Packaging:  In RF-shielded AEC/NIM #1 module; Lemo-type connectors.

Current Requirements:  + 12 volts at 160 mA
  + 6 volts at 240 mA
  - 6 volts at 490 mA
  - 1 2 volts at 195 mA
  -24 volts at 80 mA
```

---

# 623B Octal, 100 MHz Discriminator
# 821 Quad, 100 MHz Discriminator
# 4608C Octal, 150 MHz Discriminator *(Note - the 4608C is no longer available)*

- NIM Packaging
- High Speed
- Variable Threshold and Output Width Per Channel
- Good Stability
- No Multiple Pulsing

**GENERATION OF LOGIC PULSES FROM ANALOG SIGNALS**

A discriminator generates precise logic pulses in response to its input exceeding a given threshold. Output pulses are of standard amplitude and of preset duration or proportional to the input rate. The threshold is a specific voltage of interest to the user (which can be set above some critical noise level or correspond to a physical quan tity such as energy). In other applications, the threshold level can correspond to a certain level of integrated rates (coincidence events).

The output of a discriminator can be used to trigger or gate associated portions of the data collection system or to generate pulses which are to be counted. It may also be integrated into a complex logic system allowing sophisti cated decisions to be made in real time.

LeCroy's family of NIM discriminators offers flexibility and versatility with features such as at least three outputs per channel, adjustable output width and variable threshold level settings. The low minimum threshold levels permit the use of lower gain photomultipliers, long input cables and often avoid the need for preamplifiers.

# FUNCTIONAL DESCRIPTION

LeCroy's NIM discriminators offer versatility, high speed, multiple input and high performance packaged in single -width NIM modules. All models have small double pulse resolution times and have updating capabilities to reduce dead time. Input signal threshold levels as well as output pulse widths are fully adjustable over a wide range for each channel. Each module offers at least three outputs per channel for added convenience and has a maximum counting rate exceeding 100 MHz. In addition, a common Veto or Inhibit is provided.

Each module offers a variable threshold from -30 mV (-15 mV for the Model 4608C) to -1 V via a front-panel screwdriver adjustment for each channel. The low threshold level is useful when working with signals directly from photomultipliers and other detectors. A monitor point is provided to permit measurement of the threshold level with a voltmeter, assuring accurate results even in varied operating environments. Threshold stability is 0.3%/°C or better. Low input reflections make these units less sensitive to multiple pulsing.

The Model 623B and the Model 821 operate at maximum rates of 100MHz while the Model 4608C operates up to 150 MHz. All modules have updating capability which permits retriggering while an output from a previous input is still present. A second pulse, which exceeds threshold while an output is already occurring extends the present output by the preset width. However, if the second threshold crossing occurs within the double pulse resolution time, the module will not respond. This configuration is useful when the discriminators are used in DC coincidence logic.

The 821 and 4608C have a selectable Burst Guard operation. In this mode, the output is extended until the falling edge of the last pulse of the burst when input pulses are separated by less than the resolving time. This feature is particularly important when the module is used in Veto applications.

Although the actual width depends on the rate of input and the mode of operation, outputs of the modules are NIM Standard (see Application Note AN-34) level signals with minimum widths set by the front-panel controls. There are a minimum of three standard negative NIM outputs per channel. In addition, the 821 and the 4608C both have one complementary output per channel.

The 4608C includes a built-in test feature which simulates an input signal for each channel. The test feature is enabled with the receipt of a NIM level applied to the front-panel Lemo connector and permits rapid simultaneous testing of all channels.

# SPECIFICATIONS

## Model 821

### INPUT

**Signal Inputs:** Four inputs via Lemo connectors, 50 ohm ±5% protected to ±5 A for 0.5 µsec, clamping at +1 and -7V. Reflections: < 1% for input pulses of 3nsec rise time. Offset 0 ±2 mV.

**Threshold:** -30mV to -1.0 V; front-panel screwdriver adjustment. Stability: 0.2%/°C over 20°C to 60°C operat ing range. Threshold Monitor has 10:1 ratio of monitor voltage to actual voltage, ±5%. Hysteresis: 15 mV.

**Veto:** Front-panel connector permits simultaneous inhibiting of all channels; 50 ohm; requires NIM-level signal; direct-coupled, must overlap leading edge of input signal. Must precede input by approximately 5 nsec to inhibit. Minimum width 5nsec.

**Bin Gate:** Slow gate via rear connector and rear-panel ON-OFF switch; rise times and fall times approximately 50 nsec; clamp to ground from +5 inhibits; direct-coupled.

### OUTPUT

**Negative Outputs:** Two bridged pairs (0 mA quiescently, -32 mA during output). Amplitude limit of -1.2 V. Rise time < 2.0 nsec, fall time < 2.5 nsec typical but slightly longer on wider output durations. Width Stability is < ±0.2%/°C maximum. Duration of output depends on mode of operation selected by front panel switch.

*Update Only Mode:* 5 nsec to 1 µsec, continuously variable up to 600 nsec with a setting for 1 µsec via front -panel screwdriver control. (Narrower widths possible at slight expense of amplitude.)

*Burst Guard Mode:* Output duration is either equal to the time-over-threshold of the input signal or equal to the preset duration, whichever is greater. For input burst rates greater than the DPR of the unit, the output is equal to the duration of the burst.

**Fast Negative Timing Output:** Differential type current source (0 mA quiescently, -16 mA in 50 ohm during output). Rise time is typically 1.5 nsec.

**Complementary Output:** As above except levels opposite.

**GENERAL**

**Maximum Rate:** 110 MHz typical, input and output.

**Double Pulse Resolution:** < 9 nsec.

**Time Slewing:** < 1 nsec for input amplitudes 110% of threshold and above.

**Input-Output Delay:** 9.5 nsec, typical.

**Multiple Pulsing:** None; one and only one output pulse of preset duration is produced for each input pulse regardless of input pulse amplitude or duration.

**Rate LED:** One per channel. Indicates discriminator output; 10 msec stretching.

## Model 4608C

**INPUT**

**Signal Inputs:** Eight inputs via Lemo front-panel connectors, 50 W ±5% protected to ±5 A for 0.5 µsec clamping at ±5 V. Reflections: < 4% for input pulses of 2 nsec rise time.

**Threshold:** -15 mV to -1 V ±2.5 mV or ±5%, whichever is greater. Stability: better than 0.3%/°C to 60°C operat ing range. Offset ±3mV. Threshold Monitor: front-panel test point has 10:1 ratio of monitor voltage to actual voltage ±5%. Hysteresis: Typical 3.5mV.

**Test Input:** One NIM input via a Lemo connector on the front-panel, 50 ohm ±5%, triggers all channels. Minimum width: 3 nsec. Maximum rate: 150 MHz.

**Veto Input:** One NIM input via a Lemo front-panel connector, 50 W ±5%, permits simultaneous fast inhibiting of all channels. Must precede input signal by approximately 1nsec and overlap its leading edge in Update Mode or completely overlap input signal in Burst Guard Mode. Minimum duration: 3 nsec.

**OUTPUT**

**Negative Outputs:** Three outputs, NIM (0 mA quiescently, -50 mA ±6 mA during output, -800 mV into three 50 W loads). Amplitude limited to -1.2 V. Duration 4.5 nsec to > 100 nsec. Rise times and fall times less than 2 nsec. Width stability better than 0.3%/°C, 821, 4608C max.

**Complementary Output:** One output, NIM (16 mA ±2mA quiescently, 0mA during output). Duration, rise times, fall times, and width stability specifications are identical to those of negative outputs.

*Veto Input to 4608C with Updating and Burst Guard Operations Diagram.*

**GENERAL**

**Maximum Rate:** 150 MHz.

**Double Pulse Resolution:** Typical, 5 nsec.

**Time Slewing:** 500 psec for input amplitudes from

2x to 20x over threshold.

**Input-Output Delay:** < 18 nsec.

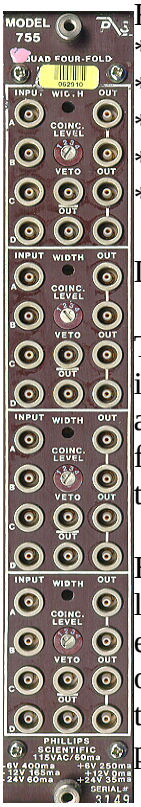
**Test-Output Delay:** < 18 nsec.

**Multiple Pulsing:** None, one and only one output pulse is produced for each input pulse regardless of input pulse amplitude and duration.

**Burst Guard:** A front-panel switch enables the Burst Guard or Updating operation for all channels.

*Comparison of Updating and Burst Guard Modes with various fast input signals. DPR is the Double Pulse Resolution.*

## PHILLIPS 755 QUAD 4 FOLD LOGIC UNIT




FEATURES
* VERSATILE LOGIC MODULE WITH MAJORITY LEVEL SELECTION
* FOUR INDEPENDENT CHANNELS
* 125 MHz RATE CAPABILITY
* DEADTIMELESS UPDATING OUTPUTS
* FAST ANTI-COINCIDENCE CAPABILITY

DESCRIPTION

The model 755 logic unit contains four channels of four input logic with veto in a single width NIM module. Logic AND, OR majority logic, fan-in/fan-out, and anti-coincidence functions can be performed with this versatile module. All functions are direct coupled and operate to over 125 MHz with input overlap times as narrow as 1 nSEC.

Each channel has four logic inputs, an anti-coincidence input, a coincidence level switch, and five outputs with common width control. The inputs are enabled by connecting the input cable to the desired input, eliminating errors often occuring with switched inputs. The setting of the coincidence level switch then determines whether a logic OR, AND, or majority logic function will produce an output.

After the inputs have satisfied the logic function desired, triggering of an updating regenerative stage produces a standard- ized output pulse, variable from 4 nSEC to 1 uSEC, independent of the input pulse shapes or overlap times. The updating feature ensures deadtimeless operation, while the double-pulse resolution is 7.5 nSEC for fast counting applications.

The outputs are the current source type with two pairs of negative bridged outputs and one complement for each channel. \X/hen only one output of a bridged pair is used, a double-amplitude NIM pulse (-32 mA) is generated for driving long cables with narrow pulse widths. The outputs have transition times of typically 1.0 nSEC, and their shapes are virtually unaffected by the loading conditions of the other outputs.

INPUT CHARACTERISTICS

A, B, C, D,
Four inputs per section, LEMO connectors; accepts NIM level logic signals (-500 mv); 50 ohm input impedance direct coupled; input reflections are less than +/-5% for a 1 nSEC rise-time. Inputs are protected against damage from +/-50 volt input transients. Inputs respond to a 1 nSEC or greater input width.

Fast Veto,
One input per section, LEMO connector; accepts NIM level logic signal (-500 mV); 50 ohm input impedance, direct coupled; less than +/-5% input reflection for a 1 nSEC risetime, protected against damage +/-50 volt input transients. Requires a 3.5 nSEC minimum input width in time with the input pulse leading edge to inhibit.

Bin Gate,
Rear-panel slide switch enables or disables the slow bin gate via the rear connector. Signal levels are in accordance with the TID-20893 standard.

INPUT CHARACTERISTICS

General
Five outputs per section, two pairs of negative bridged and one complemented NIM. The two pairs of bridged outputs are quiescently 0 mA and -32 mA during output. (-1.6 V into 50 ohms or -.8 V into 25 ohms). The complemented output is quiescently -16 mA and 0 mA during output. Risetimes and falltimes are less than 1.5 nSEC, and the output pulse shapes are optimized when the bridged outputs are 50 ohm terminated.

Width Control
One control per section; 15-tum screwdriver adjustment. Outputs are continuously variable from 4 NSEC to 1 uSEC; better than 0.15%/OC.

Updating Operation:
The output pulse will be extended if a new input pulse occurs while the output is active. This provides deadtimeless operation and 100% duty cycle can be achieved.

GENERAL PERFORMANCE

Functions:
Logic AND, OR, majority logic, and logic fan-in/fan-out. All functions have leading edge inhibit with standard-ized outputs.

Rate:
150 MHz minimum, input to output. Typically 160 MHz.
Double-Pulse Resolution:
Less than 6.5 NSEC; Typically 6 NSEC with output width set at minimum.
Input to Output Delays
Less than 8 NSEC.
Multiple Pulsing:
One and only one output pulse regardless of input pulse amplitude or duration.
Power Supply Requlrements:
-6 V @ 400 mA +6 V @ 250 mA
-12 V @ 165 mA +12 V @ 0 mA
-24 V @ 60 mA +24 V @ 35 mA
115 VAC @ 60 mA
Note All currents within NIM specifications limits allowing a full-powered bin to be
operated without overloading.
Operating Temperature#
O'C to 70'C ambient.
Packaging:
Standard single width NIM module in accordance with TID-20893 and Section 524.
Options#
Call Phillips Scientific to find out about available options.

# 705 Octal Discriminator

## FEATURES

- Individual Threshold and Width Controls
- Linear Summed Output
- Both Fast Veto and Bin Gate
- Low Cost
- Eight Channels in Single Width Module

## DESCRIPTION

The Model 705 was specifically designed for modern experiments with large counter arrays, offering high performance and reliability at a reasonable cost. The 705 features eight (8) totally independent channels with individual threshold and width controls. In addition, a fast veto input and a summed output are common to all channels.

Each channel has a threshold adjustment continuously variable from -10 mV to -1 Volt with a front panel test point providing a DC voltage ten (10) times the actual threshold setting. Likewise, each channel has a non-updating regeneration circuit for adjustable output widths from 6 nSec to 150 nSec.

A unique summed output is common to all eight channels providing -1 mA of current for each activated channel, thus allowing a fast decision to be made on the number of channels simultaneously hit. Up to 16 channels can be "OR'D" directly by cable to other summed outputs allowing a versatile scheme to form a trigger.

A fast veto input allows simultaneous inhibiting of all channels to reject unwanted events early in the system. Similarly, a bin gate will inhibit the entire module when applied via the rear connector.

The outputs are the current source type with one pair of negative bridged outputs and one complement for each channel. When only one output of the bridged pair is used, a double-amplitude NIM pulse (-32mA) is generated, when both connectors are used normal NIM levels (-16mA) are produced. The outputs have crisp, clean transitions, and their shapes are unaffected by the loading conditions of the other outputs.

# 706 Leading Edge Discriminator

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## FEATURES

- Sixteen Channels in Single Width NIM Module
- 100 MHz Input to Output Rate
- Common Threshold Control -10 mV to -1 Volt
- Common Width Control 5 nS to 150 nS
- Fast Common Veto and Bin Gate
- Non-Updating Outputs
- One Pair Bridged Outputs per Channel
- Reliable Current-Switched Outputs

## DESCRIPTION

The Model 706 is a 100 MHz Leading Edge Discriminator specifically designed for experiments with large counter arrays, offering high performance and reliability at a reasonable cost. The 706 features sixteen channels with common threshold and width controls. In addition, a fast veto input and a Bin Gate are common to all channels.

The 706 has high input sensitivity of -10mV variable to -1Volt via a 15-turn front panel control. A front panel test point provides a DC voltage equal to the actual threshold to insure accurate settings. Likewise, output durations are continuously variable via a front panel control over the range of 5nSec to 150nSec. The 706 employs non-updating regeneration circuits for output widths that are always the same duration regardless of the input rate conditions.

A fast veto input allows simultaneous inhibiting of all channels to reject unwanted events early in the system. Similarly, a bin gate will inhibit the entire module when applied via the rear connector.

The outputs are the current source type with one pair of negative bridged outputs for each channel. When only one output from the bridged pair is used, a double-amplitude NIM pulse (-32mA) is generated useful for driving long cables with narrow pulses. Two normal NIM levels are produced when both of the bridged outputs operate into 50 ohm loads. The output risetimes and falltimes are typically 1.5nSec, and their shapes are unaffected by the loading conditions of the other outputs.

## MODEL 740 QUAD LINEAR FAN-IN/FAN-OUT

FEATURES
Four Independent Channels
Linear or Logic Fan-In of Four and Fan-Out of Six per Channel
Wideband - DC to 250 MHz
Fully Bipolar Operation to +/-2.5 Volts
DC Offset Control per Channel of +/-500 mVolts
Reliable - Both Inputs and Outputs are protected

DESCRIPTION

'Me Model 740 is a four channel, unity gain linear or logic fan-in/fan-out packaged in a single width NIM module. Four linear inputs allow summing of linear levels or pulses. Both inverted and noninverted output levels are produced simultaneously allowing very complex triggers to be fast and easy to develop. Direct coupling of all inputs and outputs eliminates the baseline shifts due to rate or duty cycle affects, while making the device useful for per- forming logic functions.

```
 INPUT CHARACTERISTICS
 general        Four LEMO connectors per channel, bipolar input;
accepts
          positive or negative voltages.

 Impedance       50 ohms +/-2%, direct coupled input.

 Protection       Protected with clamping diodes, no damage will occur
from
          transients of +/-100 Volts (+/-2 amps) for 1 usec or less
duration.

 Reflections       Less than +/-4% for input risetime of 1 nsec.

 Overdrive Response     Recovery time of 20 nsec for a +/-10 Volt
input.

 OUTPUT CHARACTERISTICS
 General        Six bridged LEMO output connectors per channel. Four
non-
          inverted outputs and two inverted outputs-, low impedance
          voltage source output stage.

 Protection       Outputs can be continuously shorted to ground without
suffer-
          ing damage.

 Output Voltage Swing     Bipolar outputs deliver over +/-2 Volts
across four 50 ohm
          loads.
```

DC Offset A front panel 15-turn potentiometer provides +/-500 mvolt adjustment. A front panel test point allows easy monitoring of the DC offset.

GENERAL PERFORMANCE

Gain Fixed gain of 1.0 +/-2% both inverted and noninverted.

Stability Better than +/-50 uVolt/'C from DC to 1 mHz, and +/-.05%/'C above 1 MHz.

Linearity +/-0.2% for +/-2 Volts across two 50 ohms loads or +/-1.5 Volts across four 50 ohm loads.

Bandwidth DC to 250 MHz, 3 db point 1 Volt peak to peak.

Wideband Noise Less than 400 uvolts RMS, referred to the input (15 nV/Hz^.5).

Risetime Typically 1. 3 nsec, for a 1 Volt output excursion.

Crosstalk Greater than 60 db, DC to 100 MHz.

Power Supply Requirements +6V @ 350 mA +12V @ 160 mA -6V @ 350 mA -12V @ 160 mA

NOTE: All currents within NIM specification limits allowing full powered bin to be operated without overloading .

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# 417 NIM Pocket Pulser

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## FEATURES

- Current Switching NIM Output Pulse
- Operates Direct Coupled into 50 Ohm Load
- Long Battery Life - Three Years
- 6nSec Pulse Width *at* 10 KHz *Rate*
- Small Size - Low Cost

## DESCRIPTION

The NIM pocket pulser is a compact, lightweight battery operated pulse generator. It provides a convenient and portable way of simulating fast negative photomultiplier pulses or NIM logic pulses, to easily check cables and electronics in the laboratory or remote experimental sites. The model 417 generates a negative pulse resembling a photomultiplier with the risetime of 1.5nsec and width of 6nSec at a 10 KHz rate. An output is present when a load of 10 Kohms or less is connected. With no load the pulser goes to a standby condition with a battery life in excess of three years. The fully compatible fast NIM output is typically -16mA (-800mVolts across 50 ohms), with no DC offset present. The current switching output will not be damaged when testing shorted cables.

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# 2415 HIGH VOLTAGE POWER SUPPLY

- ±3.5 or ±7 kV Scales
- 14-Bit CAMAC Voltage Programming
- ADC Voltage/Current Monitor
- 8-Bit Current Limit CAMAC Programming

## FOR GENERAL PURPOSE LABORATOR APPLICATIONS

The Model 2415 is a versatile, general purpose high voltage power supply packaged in a #2 CAMAC module. The output voltage and the maximum output current can be set via front-panel multi-turn potentiometers or CAMAC programming. The front-panel voltage and current settings serve as hardware limits for the CAMAC demand values. This feature eliminates the possibility of detector damage due to inadvertent software errors or computer failures. The unit offers front-panel BNC voltage and current monitor outputs. A built-in ADC allows both to be read via CAMAC.

The 2415 offers circuit-board mounted jumpers which allow the unit to be operated in several modes. One set of jumpers selects the output polarity. The other set selects the output range, 3.5 kV or 7 kV maximum. Front-panel LEDs indicate the mode selected. The high and low level outputs are provided at separate output connectors.

When used in the ±3.5 kV ranges, the 2415 offers 0.25 V CAMAC voltage programming resolution with a voltage monitor resolution of 1 V. It provides an output current of up to 2.5 mA with current monitor resolution of 0.625 µA. When used in the ±7 kV ranges, the 2415 offers 0.5 V CAMAC voltage programming resolution with a voltage monitor resolution of 2 V. It provides an output current of up to 1.0 mA with current monitor resolution of 250 nA.

Special attention has been given to the current monitor circuitry. In the 7 kV CAMAC mode, the device can register a current of less than 1 µA.

# SPECIFICATIONS

| VOLTAGE CONTROL | ±3.5 kV Configuration | ±7 kV Configuration |
|---|---|---|
| | | |
| Range | 100-3500 V | 200-7000 V |
| CAMAC Programming | 14 bits | 14 bits |
| CAMAC Step | 0.25 V | 0.5 V |
| CAMAC Accuracy | [2] ±(1.5 V + 0.1%) | [2] ±(3 V + 0.1%) |
| Front-Panel Adjustment | Ten-turn vernier potentiometer | |
| | 500 V/turn | 1000 V/turn |
| CAMAC Monitor | 12-bit ADC | 12-bit ADC |
| CAMAC Resolution | 1 V | 2 V |
| CAMAC Offset (response to 0 V output) | 0-2 counts | 0-2 counts |
| CAMAC Accuracy | ±0.2% | ±0.2% |
| Front-Panel Monitor | Low Impedance (< 10 ohm) voltage output, suitable for driving a meter; BNC connector. | |
| Front-Panel Scale | 2 V/kV ±0.5% | 1 V/kV ±0.5% |
| Front-Panel Offset (value for 0 V output) | [2] ±4 V referred to HV output | [2] ±8 V referred to HV output |
| | | |
| **CURRENT CONTROL** | | |
| | | |
| Range | 0-2.5 mA | 0-1 mA |
| CAMAC Programming | 8 bits | 8 bits |
| CAMAC Step | 10 µA | 4 µA |
| CAMAC Accuracy | ±(1% + 12 µA) | ±(1% + 5 µA) |
| Front-Panel Adjustment | Ten-turn vernier potentiometer | |
| | 250 µA/turn | 100 µA/turn |
| CAMAC Monitor | 12-bit ADC | 12-bit ADC |
| CAMAC Resolution | 625 nA | 250 nA |
| CAMAC Offset (Response to 0 µA load) | 1 or 2 counts | 1 or 2 counts |
| CAMAC Accuracy | ±0.5% | ±0.5% |
| Front-Panel Monitor | Low Impedance (< 10 ohm) voltage output, suitable for | |

| | | |
|---|---|---|
| | driving a meter; BNC connector. | |
| Front-Panel Scale | 4 V/mA ±0.5% | 10 V/mA ±0.5% |
| Front-Panel Offset (value for 0 V output) | [2] ±4 µA | [2] ±2 µA |
| | | |
| **GENERAL** | | |
| | | |
| Output Power Rating | 7 W | 7 W |
| Output Ripple (at maximum current) | < 50 mV rms | < 50 mV rms |
| Output Temperature Coefficient | Typically ±50 ppm/¡C, ±100 ppm/¡C maximum | |
| Voltage Regulation | < 0.5 V (0 to 2.5 mA) | < 1 V (0 to 1 mA) |
| Short Circuit Protection | Yes | Yes |
| Output Connector | SHV | Reynolds 1064-1 |
| | | |
| **CONTROLS** | | |
| | | |
| HV On/Off | Toggle switch; turns On/Off HV output. | |
| Manual/Remote | Selects front panel or CAMAC operation of voltage and current set. | |
| ADC | 12 bits; conversion time < 30 µsec. | |
| | | |
| **INDICATOR LAMPS** | | |
| | | |
| HV On | Voltage present at output. | |
| Overload | Supply in current-limiting mode. | |
| Positive | Positive output configuration. | |
| Negative | Negative output configuration. | |
| 3.5 kV | ON | OFF |
| 7 kV | OFF | ON |
| | | |
| **POWER** | 350 mA at +24 V; 350 mA at -24 V; 350 mA at +6 V. | |

# CAMAC COMMANDS

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## CAMAC COMMANDS

**Z:** Clear LAM, demand voltage and current limit registers (also occurs on CAMAC power up).

**Q:** A Q = 1 signal for F(0) indicates A/D conversion complete and valid data at R1...R12. A Q = 1 signal for F(8) indicates LAM is set and an overload condition has occurred since the last F(10).

**X:** An X = 1 (command accept) is generated when a valid N, F command is received. (Some commands which are acknowledged by X have null function. Validity of A is not taken into account.)

**L:** A Look-At-Me signal (if enabled by on-board jumper) indicates an overload condition has oc curred since the last F(10). L is inhibited when module is addressed.

## CAMAC FUNCTION CODES

**F(0):** Read ADC data via R1...R12. A Q = 1 response indicates ADC conversion is complete, and data on R1...R12 is valid.

**F(8):** Test LAM. Q = 1 if the LAM is true.

**F(10):** Clear LAM. (LAM is set by overload condition.)

**F(16)·A(0):** Write demand voltage via W1...W14.

**F(16)·A(1):** Write current limit via W1...W8.

**F(26)·A(0):** Convert output voltage to digital value. Read by a subsequent F(0) command.

**F(26)·A(1):** Convert output current to digital value. Read by a subsequent F(0) command.

# AN INTRODUCTION TO CAMAC

Computer Automated Measurement And Control, (CAMAC), is a modular data handling system used at almost every nuclear physics research laboratory and many industrial sites all over the world. It represents the joint specifications of the U.S. NIM and the European ESONE Committees.

The primary application is data acquisition but CAMAC may also be used for remotely programmable trigger and logic applications (LeCroy ECLine family of programmable logic units). The CAMAC standard covers electrical and physical specifications for the modules, instrument housings or crates, and a crate backplane. Examples of crates include the LeCroy Model 8025 with 25 positions and the Model 8007 with 7 positions.

Individual crates are controlled by slave or intelligent controllers. The controllers are tied together with a parallel Branch Highway that ends in a Branch Driver. The Branch Driver is interfaced directly to a data acquisition computer. Alternatively, tree or parallel data acquisition architectures may be created by connecting secondary CAMAC branches via CAMAC Branch Driver Modules.

CAMAC crates may also be connected in a Local Area Fiber Optic Network via the LeCroy Model 5211A Fiber Optic Serial Link and a serial crate controller. Up to 62 crates separated by a maximum of 500 m can exchange data at transmission rates of 45 megabytes/sec.

LeCroy also offers crate controllers that interface directly with the GPIB or IEEE Std. 488-1978 Bus. Therefore, an entire CAMAC Crate may appear as a single instrument on this very popular laboratory instrument bus. The Model 8901A is a GPIB/CAMAC slave interface that operates as a "Talker/Listener".

Timing and protocol specifications permit up to 1 megaword/sec transfers of 16 or 24-bit words for both the Dataway and CAMAC Branch. GPIB timing is usually limited by the host computer and typically runs at 500 kilobytes/sec.

## INTRODUCTION

CAMAC is an international standard of modularized electronics as defined by the ESONE Committee of the JRC, Ispra. Its function is to provide a scheme to allow a wide range of modular instruments to be interfaced to a standardized backplane called a DATAWAY. The DATAWAY is then interfaced to a computer. In this way, additions to a data acquisition and control system may be made by plugging in additional modules and making suitable software changes. Thus, CAMAC allows information to be transferred into and out of the instrument modules.

CAMAC modules may be plugged into a CAMAC crate which has 25 STATIONS, numbered 1 - 25. Station 25, the rightmost station, is reserved for a CRATE CONTROLLER, whereas Stations 1 - 24 are NORMAL STATIONS used for CAMAC

modules (see Block Diagram). Usually, Station 24 is also used by the controller in that most controllers are double width (#2 CAMAC). The purpose of the controller is to issue CAMAC COMMANDS to the modules and transfer information between a computer (or other digital device) and the CAMAC modules.

Module power, address bus, control bus and data bus are provided by the DATAWAY. The DATAWAY lines include digital data transfer lines, strobe signal lines, and addressing lines and control lines. See Table 3 for a pin allocation chart.

In a typical DATAWAY operation, the crate controller issues a CAMAC COMMAND which includes a station number (N), a subaddress (A), and function code (F), (see Table 1). In response, the module will generate valid command accepted (X response) and act on the command. If this command requires data transfer, the (R) or write (W) line will be used. Note that the terms Read and Write apply to the controller, not the module. For example, under a Read command, the controller reads data contained within a module.

**USE OF THE DATAWAY**

Communication with plug-in units takes place through the DATAWAY. This passive backplane is incorporated in the crate and links the 86-pin sockets to all stations. The bus lines link corresponding pins at all normal stations and, in some cases, the control station. Individual lines link one pin at a normal station to one pin at the control station. The patch pins have no specified DATAWAY wiring but can be connected to individual points to which patch leads may be attached.

During a DATAWAY operation the controller generates a command consisting of signals on individual Station Number lines to specify one or more modules, signals on the Subaddress bus lines to specify a sub-section of the module or modules, and signals on the Function bus lines to specify the operation to be performed. The command signals are accompanied by a signal on the Busy bus line, which is available at all stations to indicate that a DATAWAY operation is in progress.

When a module recognizes a Read command calling for a data transfer to the controller, it establishes data signals on the Read bus lines. When a controller recognizes a Write command calling for a data transfer to a module, it establishes data signals on the Write bus lines. In addition, regardless of whether there is transfer on the R or W lines, the module may transmit one bit of status information on the Response bus line.

Two timing signals, Strobes S1 and S2, are then generated in sequence on separate bus lines. The strobes are used to transfer data from the DATAWAY into modules (on Write commands) and into the controller (on Read commands). They may also initiate other actions within the controller and modules. Whenever there is no DATAWAY operation in progress (indicated by the absence of the Busy signal) any module may generate a signal on its individual Look-at-Me line to indicate that it requires attention. Three common control signals are available at all stations, without requiring addressing by a

command, in order to initialize all units (typically after switch-on), to Clear data registers, and to inhibit features such as data-taking.

**Definition of Commands**

A command consists of signals on the DATAWAY lines which specify at least one module (by individual station number lines), a subsection of the module or modules (by the four subaddress bus lines), and the function to be performed (by the five function bus lines). The command signals are maintained for the full duration of the operation on the DATAWAY. They are accompanied by a signal on the Busy bus line which indicates to all units that a DATAWAY operation is in progress.

**STATION NUMBER (N)**

Each normal station is addressed by a signal on an individual station number line (N) which comes from a separate pin at the control station. The stations are numbered in decimal code from the left-hand end as viewed from the front, beginning with Station 1.

**SUBADDRESS (A8, A4, A2, A1)**

Different sections of a module are addressed by signals on the four A bus lines. These signals are decoded in the module to select one of up to sixteen subaddresses, numbered in decimal from 0 to 15.

**FUNCTION (F16, F8, F4, F2, F1)**

The function to be performed at the specified subaddress in the selected module or modules is defined by the signals on the five F bus lines. These signals are decoded in the module to select one of up to 32 functions, numbered in decimal from 1 to 31. The definitions of the 32 function codes are summarized in the DATAWAY Command Operations section.

**STROBE SIGNALS (S1 AND S2)**

Two strobe signals S1 and S2 are generated in sequence on separate bus lines. These signals are used to transfer information between plug-in units via the DATAWAY or to initiate operations within units. In either case the specific action is determined by the command present on the DATAWAY. Both strobes are generated during each DATAWAY command operation, and all plug-in units which accept information from the DATAWAY do so in response to these strobes. The first strobe S1 is used for actions which do not change the state of signals on the DATAWAY lines. All units which accept data from the DATAWAY in a Read operation, or in a Write operation do so in response to S1. The second strobe S2 is used to initiate any actions which may change the state of DATAWAY signals, for example, clearing a register whose output is connected to the DATAWAY.

**Data**

Up to 24 bits of data may be transferred in parallel between the controller and the selected module. Independent lines (Read and Write) are provided for the two directions of transfer.

**THE WRITE LINES (W1-W24)**

The controller or other common data source generates data signals on the W bus lines at the beginning of any "Write" operation. The W signals reach a steady state before S1, and are maintained until the end of the operation, unless modified by S2.

**THE READ LINES (R1-R24)**

Data signals are set up on the R bus lines by the module as soon as a "Read" command is recognized. The R signals reach a steady state before S1, and are maintained for the full duration of the DATAWAY operation, unless the state of the data source is changed by S2. The controller or other common data receiver strobes the data from the R bus lines at the time of the Strobe S1.

**Status Information**

Status information is conveyed by signals on the Look-at-Me (L), Busy (B), Command Accepted (X) and Response (Q) lines.

**LOOK-AT-ME (L)**

This, like the N line, is an individual connection from each station to a separate pin at the control station. When there is no DATAWAY operation in progress (no B present) any plug-in unit may generate a signal on its L line to indicate that it requires attention. When B is present each L signal is gated off the DATAWAY line by the unit which generates it.

A Look-at-Me request can be reset by Clear Look-at-Me, initialize, or by the performance of the specific action which generated the request.

**DATAWAY BUSY (B)**

The Busy signal is used to interlock various aspects of a system which can compete for the use of the DATAWAY. Specifically, it is generated during DATAWAY command or common control operations. Whenever N is present, B is present, and for the duration of B, all L signals are gated off the DATAWAY lines.

**COMMAND ACCEPTED (X)**

Whenever an addressed (N = 1) module recognizes a command, it must generate X = 1.

**RESPONSE (Q)**

The Q bus line is used during a DATAWAY operation to transmit a signal indicating the status of a selected feature of the module. On all Read and Write commands the signal on the Q bus line remains static from the time the command is received until S2. For all other commands the signal on the Q bus line may change at any time.

**Common Controls**

Common control signals operate on all modules connected to them without the need to be addressed separately by a command. In order to provide protection against spurious signals, the initialize (Z) and Clear (C) signals must be accompanied by Strobe S2.

**INITIALIZE (Z)**

The initialize signal has absolute priority over all other signals or controls. It sets all units to a basic state by resetting all registers, whether data or control, to a defined state, and by resetting all L signals and disabling them where possible. Units which generate Z must also cause S2 and B to be generated. Modules which accept Z gate it with S2 as a protection against spurious signals on the Z line.

**INHIBIT (I)**

The presence of this signal inhibits any activity (for example, data taking). It must either not change when B is present or have rise and fall times not less than 200 nsec.

**CLEAR (C)**

This command signal clears all registers or bistables connected to it. Units which generate C must also cause S2 and B to be generated. Modules which accept C gate it with S2 as a protection against spurious signals on the C line.

**Private Wiring**

**PATCH LEADS (P1-P7)**

Five pins (P1 to P5) on the 86-way socket at normal stations are not prewired to DATAWAY lines but are freely available for local connections. At the control station, seven pins (P1-P7) are available.

**Dataway Command Operations**

A Command is composed of signals on the Station Number line or lines, the Subaddress lines and the Function lines. It is accompanied by a signal on the Busy Line. In response to a command, data may be transferred on the Read or Write lines and one bit of status

information on the Q line. The two Strobes S1 and S2 must be generated in each DATAWAY command operation to control its timing.

The order in which the commands are described below corresponds to the function codes set out in Table 1. In this table the term "register" is used for an addressable data source or receiver, without implying that it has a data storage property. The function codes allow the registers in a module to be divided into two distinct sets, known as Group 1 and Group 2. Thus it is possible to operate on more than the basic set of 16 registers selected by the four subaddress lines.

A common feature of all commands is that if the module has a Look-at-Me source which requests a specific command, then the performance of the command should reset the Look-at-Me source.

**READ COMMANDS (FUNCTION CODES 0-7)**

Read commands are identified by the combination F16 = 0, F8 = 0 in the function code. They specify that information is to be transferred from a module to a controller via the R bus lines. Data signals are set up on the R bus lines by the module as soon as the "Read" command is decoded, and the appropriate status signal connected to the Q bus line. The R and Q signals must reach a steady state before S1, and are maintained for the full duration of the DATAWAY command operation unless the state of the signal source is changed at S2. The controller or other common data receiver strobes the data from the R and Q bus lines at the time of the Strobe S1.

In order to facilitate reading by sequential addressing, all registers containing data (as opposed to control information) must have consecutive subaddresses starting at subaddress 0. At each of these subaddresses the module generates Q = 1 in response to the appropriate Read command. At the next subaddress in sequence (where there is not a data register) the response is Q = 0. At all remaining addresses the Q signal may be used to test any feature, subject to the general requirement that the Q signal must be static from the beginning of command until at least S2.

**CODE 0, READ GROUP 1 REGISTER**

This command selects, by subaddress, one register from the first group in the module and transfers the contents of this register to the controller. The contents of the register remain unchanged.

**CODE 1, READ GROUP 2 REGISTER**

Same as Code 0, except command selects register from the second group.

**CODE 2, READ AND CLEAR GROUP 1 REGISTER**

Same as Code 0, except the module register is cleared at time S2.

**CODE 3, READ COMPLEMENT OF GROUP 1 REGISTER**

Same as Code 0, except command transfers the complement of the contents of this register to the controller.

**CODE 4-7**

Unassigned at this time.

**Control Commands (Function Codes 8-15)**

Control Commands are identified generally by F8 = 1 in the function code. They are divided onto two groups by the state of F16, in this case F16 = 0. They specify that information is not transferred on either the R or W bus lines. However, information may be conveyed on the Q bus line in any of these commands. The signal on the Q bus line may change at any time but is strobed into the controller at time S1 and may (except in Code 8) be reset by Strobe S2.

**CODE 8, TEST LOOK-AT-ME**

This command selects a Look-at-Me source in the module and presents the state of this source on the Q bus line.

**CODE 9, CLEAR GROUP 1 REGISTER**

This command selects, by subaddress, a register from the first group in the module and clears the contents of this register.

**CODE 10, CLEAR LOOK-AT-ME**

Same as Code 8, except the Look-at-Me source is cleared at time S2.

**CODE 11, CLEAR GROUP 2 REGISTER**

Same as Code 9, except command selects register from the second group.

**CODE 12-15**

Unassigned at this time.

**Write Commands (Function Codes 16-23)**

Write commands are identified by the combination F16 = 1, F8 = 0 in the function code. They specify that information is to be transferred from a controller to a module via the W bus lines. The controller or other common data source generates data signals on the W bus lines at the beginning of the "Write" operation. The module connects the appropriate

status signal to the Q bus line as soon as the command is recognized. The W and Q signals reach a steady state before S1 and are maintained for the full duration of the DATAWAY command operation unless the status of the signal source is changed at Strobe S2. In order to facilitate writing into registers by sequential addressing, all registers which are to contain data (as opposed to control information) have consecutive subaddress starting at subaddress 0. At each of these subaddresses, the module generates Q = 1 in response to the appropriate Write function. At the next subaddress in sequence (where there is not a data register), the response is Q = 0. At all remaining subaddresses the Q signal may be used to test any feature subject to the general requirement that the Q signal must be static from the beginning of the command until at least S2.

**CODE 16, OVERWRITE GROUP 1 REGISTER**

This command selects, by subaddress, one register in the first group in the module and sets the contents of this register to correspond with the data generated on the W bus lines by the controller.

**CODE 17, OVERWRITE GROUP 2 REGISTER**

Same as Code 16, except command selects a register in the second group.

**CODE 18, SELECTIVE OVERWRITE GROUP 1 REGISTER**

Same as Code 16, except a separate "mask" register defines which bits in the selected register are set.

**CODE 19, SELECTIVE OVERWRITE GROUP 2 REGISTER**

Same as Code 18, except command selects a register in the second group.

**CODE 20-23**

Unassigned at this time.

**Control Commands (Function Codes 24-31)**

Control commands are identified generally by F8 = 1 in the function code. They are divided into two groups by the state of F16, in this case F16 = 1. They specify that information is not transferred on either the R or W bus lines. However, information may be conveyed by the Q bus line in any of these commands. The signal on the Q bus line is permitted to change at any time but is strobed into the controller at time S1 and may (except in Code 27) be reset by Strobe S2.

**CODE 24, DISABLE**

This command selects, by subaddress, and disables a feature of the module; e.g., a Look-at-Me source or a data input.

**CODE 25, INCREMENT PRESELECTED REGISTERS**

This command adds one simultaneously to the contents of each register in one of 16 groups, defined by the subaddress.

**CODE 26, ENABLE**

This command enables the feature of the module selected by the subaddress, e.g., a Look-at-Me source or a data input.

**CODE 27, TEST STATUS**

This command selects, by subaddress, any feature of a module other than a source of a Look-at-Me request and tests it by producing a response on the Q bus line.

**CODE 28 - 31**

Unassigned at this time.

**Digital Signal Standards on the Dataway**

The potentials for the binary digital signals on the DATAWAY lines have been defined to correspond with those for compatible current sinking logic devices (e.g., the TTL and DTL series). The signal convention has, however, been inverted to be negative logic. The high state (more positive potential) corresponds to logic "0" and the low state (near ground potential) corresponds to logic "1". Intrinsic OR outputs are thus available from the manufacturers' standard product range, and disconnected inputs go to the "0" state.

It is an essential feature of the DATAWAY that many units may have their signal outputs connected to the Read and Response lines. Outputs onto these lines therefore require intrinsic OR gates. The same principle is extended to other lines (Command, Write, etc.) in order to allow more than one control-line unit in a crate. The inhibit line may be an exception, since its signals are shaped with a slow rise and fall if they change during DATAWAY operations.

**VOLTAGE STANDARDS FOR DATAWAY SIGNALS**

All DATAWAY Signals must conform to the voltage levels as follows:

Pull-up current sources for all DATAWAY bus lines are located in the crate controller (occupying the control station and at least one other station) so as to insure that there is

one and only one current source per line. The minimum pull-up current when the DATAWAY line is at +3.5 V is defined as 2.5 mA. If the controller generated DATAWAY signals at time intervals near the permitted minima, the pull-up current sources should preferably provide not less than 6 mA when the lines are at this potential. The pull-up for the N signals is located in the unit generating the signals, and for the L signals in the unit receiving the signals, so that the individual lines may be joined or grouped within these units if desired.

The N and L lines are effectively individual lines joining two units (a module and a controller). The Q and R lines generally will have many units generating the signals (say 20) with a few units (maximum four) receiving the signals. The remaining lines (W, A, F, S, B, Z, I, C) will have relatively few units generating each signal (often only one) with the possibility of many units receiving the signals.

**TIMING OF DATAWAY SIGNALS**

The sequence of events during a single DATAWAY operation is shown in the Timing Diagram . The shaded areas indicate the permitted variation of each signal between an ideal square signal and a signal whose transition across the appropriate signal threshold (0.8 V or 2.0 V) satisfies the conditions shown. The signal waveforms for the command and data lines apply to those lines, if any, which take up the "1" state. Other command and data lines may, of course, be in the "0" state during the operation.

The signals on the Busy line and the various signals constituting the command need not occur in exact synchronism, provided their envelope lies within the shaded areas of the diagram. Similar variation is permitted between the signals constituting the data. The broken line indicates the earliest time at which the data signals may change in response to S2.

Key points on these waveforms are indicated by t0 - t9 with the following significance:

Points t0, t3, t6 represent the initiation of the negative-going of the Command, Strobe 1, and Strobe 2 signals, respectively. They are the times at which the signals would be received from an ideal DATAWAY with no capacitive loading.

Points t9, t5, t8 represent similarly the initiation of the positive-going edges of the same signals.

Points t2, t11, are the latest time at which the data source is permitted to initiate the negative-going and positive-going edges of the data signals.

Points t1, t3, t4, t7 represent the latest times at which the received signals are permitted to reach a maintained "1" state, and therefore refer to the last negative-going transition across the +0.8 V threshold.

Points t6, t9, t10, t12 represent the latest times at which the received signals are permitted to reach a maintained "0" state and therefore, refer to the last positive-going transition across the +2.0 V threshold.

Controllers must initiate the negative- and positive-going edges of the command and strobe signals at intervals not less than those defined by t3, t5, t6, t8 and t9. Modules respond to the command within the most adverse value of (t1 - t2); i.e., 100 nsec. The electrical characteristics of the DATAWAY and connections from it into units must allow signals to rise and fall within the minimum times for (t0 - t1), (t2 - t3) etc.

The next DATAWAY operation must not start before t9. The extreme case is shown in the timing diagram below with the next operation starting at t9; t9 - t12 of one operation coincides with t0 - t3 of the next. The command and data signals of one operation may thus be removed while those of the next operation are being established. The Busy signal may be maintained continuously during a sequence of consecutive DATAWAY operations. Under suitable conditions any command or data signals which have the same state during successive operations may also be maintained. In the extreme case of successive operations with the same command and data, there could be a complete absence of signal transitions between t0 and t3.

**Power Supplies**

The voltage tolerances and current loadings are specified in Table 2. The specified tolerances in voltage refer to the voltage measured at the contacts of the DATAWAY sockets and must be maintained under the worst combination of factors such as AC mains voltage and frequency, the maximum current loadings, temperature and the position in the crate of the socket under observation.

Note that the maximum currents stated in Table 2 are subject to the overall restrictions as follows:

1. The current carried by any contact of the DATAWAYsocket must not exceed 3 A.

2. The total power dissipated in a crate, without forced ventilation, must not exceed 200 W.

3. The power dissipation per single-width station should not, therefore, normally exceed 8 W. Under special circumstances, however, this rating may be increased to a maximum of 25 W, provided suitable precautions are taken to comply with total power dissipation and current loadings.

Pin Allocation at Normal Station

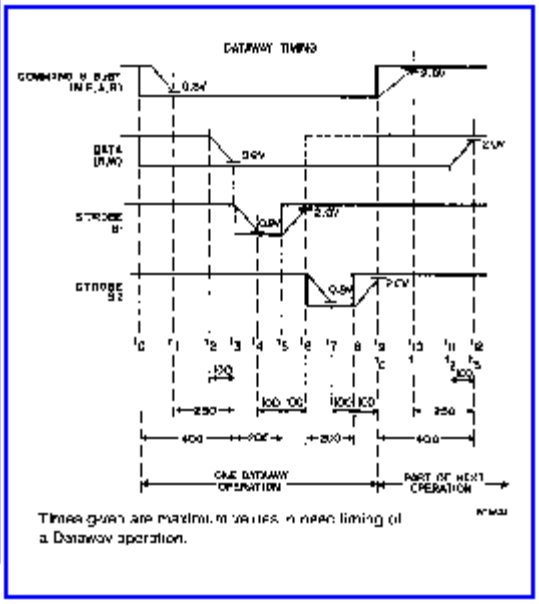
Standard Dataway Usage

## CAMAC REFERENCE DATA

### CAMAC FUNCTION CODES

| CODE F( ) | FUNCTION | FUNCTION SIGNALS F16 | F8 | F4 | F2 | F1 | CODE F( ) |
|---|---|---|---|---|---|---|---|
| 0 | Read Group 1 Register | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | Read Group 2 Register | 0 | 0 | 0 | 0 | 1 | 1 |
| 2 | Read and Clear Group 1 Register | 0 | 0 | 0 | 1 | 0 | 2 |
| 3 | Read Complement of Group 1 Register | 0 | 0 | 0 | 1 | 1 | 3 |
| 4 | Non-standard | 0 | 0 | 1 | 0 | 0 | 4 |
| 5 | Reserved | 0 | 0 | 1 | 0 | 1 | 5 |
| 6 | Non-standard | 0 | 0 | 1 | 1 | 0 | 6 |
| 7 | Reserved | 0 | 0 | 1 | 1 | 1 | 7 |
| 8 | Test Look-at-Me | 0 | 1 | 0 | 0 | 0 | 8 |
| 9 | Clear Group 1 Register | 0 | 1 | 0 | 0 | 1 | 9 |
| 10 | Clear Look-at-Me | 0 | 1 | 0 | 1 | 0 | 10 |
| 11 | Clear Group 2 Register | 0 | 1 | 0 | 1 | 1 | 11 |
| 12 | Non-standard | 0 | 1 | 1 | 0 | 0 | 12 |
| 13 | Reserved | 0 | 1 | 1 | 0 | 1 | 13 |
| 14 | Non-standard | 0 | 1 | 1 | 1 | 0 | 14 |
| 15 | Reserved | 0 | 1 | 1 | 1 | 1 | 15 |
| 16 | Overwrite Group 1 Register | 1 | 0 | 0 | 0 | 0 | 16 |
| 17 | Overwrite Group 2 Register | 1 | 0 | 0 | 0 | 1 | 17 |
| 18 | Selective Set Group 1 Register | 1 | 0 | 0 | 1 | 0 | 18 |
| 19 | Selective Set Group 2 Register | 1 | 0 | 0 | 1 | 1 | 19 |
| 20 | Non-standard | 1 | 0 | 1 | 0 | 0 | 20 |
| 21 | Selective Clear Group 1 Register | 1 | 0 | 1 | 0 | 1 | 21 |
| 22 | Non-standard | 1 | 0 | 1 | 1 | 0 | 22 |
| 23 | Selective Clear Group 2 Register | 1 | 0 | 1 | 1 | 1 | 23 |
| 24 | Disable | 1 | 1 | 0 | 0 | 0 | 24 |
| 25 | Execute | 1 | 1 | 0 | 0 | 1 | 25 |
| 26 | Enable | 1 | 1 | 0 | 1 | 0 | 26 |
| 27 | Test Status | 1 | 1 | 0 | 1 | 1 | 27 |
| 28 | Non-standard | 1 | 1 | 1 | 0 | 0 | 28 |
| 29 | Reserved | 1 | 1 | 1 | 0 | 1 | 29 |
| 30 | Non-standard | 1 | 1 | 1 | 1 | 0 | 30 |
| 31 | Reserved | 1 | 1 | 1 | 1 | 1 | 31 |

Table 1




Times given are maximum values of need timing of a Dataway operation.

## MAXIMUM CURRENT LOADS

| SUPPLY VOLTAGE | VOLTAGE TOLERANCE | IN THE PLUG-IN (PER UNIT WIDTH)* | IN THE CRATE** |
|---|---|---|---|
| **Mandatory** | | | |
| +24 V DC | ±0.5% | 1 A | 6 A |
| +6 V DC | ±2.5% | 2 A | 25 A |
| -6 V DC | ±2.5% | 2 A | 25 A |
| -24 V DC | ±0.5% | 1 A | 6 A |
| **Additional (as required)** | | | |
| +12 V DC | ±0.5% | | |
| -12 V DC | ±0.5% | | |

* See Notes 1 and 3.
** See Note 2.

Table 2

## PIN ALLOCATION AT CONTROL STATION

(STATION 25)

| | | | | | |
|---|---|---|---|---|---|
| Individual patch contact | | P1 | B | Busy | Bus line |
| Individual patch contact | | P2 | F16 | Function | Bus line |
| Individual patch contact | | P3 | F8 | Function | Bus line |
| Individual patch contact | | P4 | F4 | Function | Bus line |
| Individual patch contact | | P5 | F2 | Function | Bus line |
| Bus line | Command Accepted | X | F1 | Function | Bus line |
| Bus line | Inhibit | I | A8 | Subaddress | Bus line |
| Bus line | Clear | C | A4 | Subaddress | Bus line |
| Individual patch contact | | P6 | A2 | Subaddress | Bus line |
| Individual patch contact | | P7 | A1 | Subaddress | Bus line |
| Bus line | Strobe 1 | S1 | Z | Initialize | Bus line |
| Bus line | Strobe 2 | S2 | Q | Response | Bus line |
| | | L24 | N24 | | |
| | | L23 | N23 | | |
| | | L22 | N22 | | |
| | | L21 | N21 | | |
| | | L20 | N20 | | |
| | | L19 | N19 | | |
| | | L18 | N18 | | |
| | | L17 | N17 | | |
| | | L16 | N16 | | |
| | | L15 | N15 | | |
| | | L14 | N14 | | |
| | | L13 | N13 | | |
| 24 Individual Look-at-Me Lines | | L12 | N12 | 24 Individual Station | |
| L1 from Station 1, etc. | | L11 | N11 | Number lines | |
| | | L10 | N10 | N1 to Station 1, etc. | |
| | | L9 | N9 | | |
| | | L8 | N8 | | |
| | | L7 | N7 | | |
| | | L6 | N6 | | |
| | | L5 | N5 | | |
| | | L4 | N4 | | |
| | | L3 | N3 | | |
| | | L2 | N2 | | |
| | | L1 | N1 | | |
| | -12 V DC | -12 | -24 | -24 V DC | |
| | | NC | -6 | -6 V DC | |
| | | NC | NC | | |
| Power | Auxiliary -6 V supply | Y1 | E | Clean Earth | Power |
| Bus lines | -12 V DC | +12 | +24 | +24 V DC | Bus lines |
| | Auxiliary +6 V supply | Y2 | +6 | +6 V DC | |
| | 0 V (Power Return) | 0 | 0 | 0 V (Power Return) | |

Table 3a

## STANDARD DATAWAY USAGE

| TITLE | DESIGNATION | CONTACTS | USE AT A MODULE |
|---|---|---|---|
| **Command** | | | |
| Station Number | N | 1 | Selects the module (individual line from control station). |
| Sub-Address | A1, 2, 4, 8 | 4 | Selects a section of the module. |
| Function | F1, 2, 4, 8, 16 | 5 | Defines the function to be performed in the module. |
| **Timing** | | | |
| Strobe 1 | S1 | 1 | Controls first phase of operation. (Dataway signals may change.) |
| Strobe 2 | S2 | 1 | Controls second phase. (Dataway signals may change.) |
| **Data** | | | |
| Write | W1-W24 | 24 | Bring information to the module. |
| Read | R1-R24 | 24 | Take information from the module. |
| **Status** | | | |
| Look-at-Me | L | 1 | Indicates request for service (individual line to control station). |
| Busy | B | 1 | Indicates that a Dataway operation is in progress. |
| Response | Q | 1 | Indicates status of feature selected by command. |
| Command Accepted | X | 1 | Indicates that module is able to perform action required by the command. |

| TITLE | DESIGNATION | CONTACTS | USE AT A MODULE |
|---|---|---|---|
| **Common Controls** | | | Operate on all stations connected to them, no command required. |
| Initialize | Z | 1 | Sets module to a defined state. (accompanied by S2 and B). |
| Inhibit | I | 1 | Disables features for duration of signal. |
| Clear | C | 1 | Clears registers (accompanied by S2 and B). |
| **Non-Standard Connections** | | | |
| Free bus-lines | P1, P2 | 2 | For specified uses. |
| Patch Contacts | P3-P5 | 3 | For unspecified interconnections. No Dataway lines. |
| **Mandatory Power Lines** | | | |
| +24 V DC | +24 | 1 | |
| +6 V DC | +6 | 1 | |
| -6 V DC | -6 | 1 | |
| -24 V DC | -24 | 1 | |
| 0 V | 0 | 2 | Power return. |
| **Additional Power Lines** | | | Lines are reserved for the following power supplies. |
| +12 V DC | +12 | 1 | Low current for indicators, etc. |
| -12 V DC | -12 | 1 | Reference for circuits requiring clean earth. |
| Clean Earth | E | 1 | |
| Reserved Y1, Y2 | 2 | | Reserved for future allocation. |

Table 4

**Models Details of the Data Acquisition Setup At Panjab University Chandigarh**

| *Items* | *Model Number* | *Make* | *Address of the firm* | *Remarks* |
|---|---|---|---|---|
| **CAMAC CRATE** | MODEL 1502 | Kinetics Systems | Refer Sr. No 1 of Addresses | |
| CAMAC CRATE CONTROLLER | MODEL 3922-ZIB | Kinetics Systems | Refer Sr. No 1 of Addresses | |
| CAMAC/IBM PC Interface | Model 2927-Z1A | Kinetics Systems | Refer Sr. No 1 of Addresses | |
| !2 Channel ADC | Model 2249A | Le-Croy | Refer Sr. No 2 of Addresses | |
| TDC Module | Model 2228 A | Le-Croy | Refer Sr. No 2 of Addresses | |
| Scalar | Model 2251 | Le Croy | Refer Sr. No 2 of Addresses | |
| High Voltage Power supply | Model 2415 | Le-Croy | Refer Sr. No 2 of Addresses | |
| **NIM BIN** | Model TB 3 B | OXFORD | Refer Sr. No 5 of Addresses | |
| NIM POWER SUPPLY | Model TC 911-6 | OXFORD | Refer Sr. No 5 of Addresses | |
| Quad Majority Logic Unit | Model 755 | Phillips Scintific | Refer Sr. No 4 of Addresses | |
| Liniar Logic Fan-In-Fan-Out | Model 740 | Phillips Scintific | Refer Sr. No 4 of Addresses | |
| !6 Channel Discriminator | Model 706 | Phillips Scintific | Refer Sr. No 4 of Addresses | |
| NIM Pocket Pulser | Model 417 | Phillips Scintific | Refer Sr. No 4 of Addresses | |
| Octal Updated Discriminator | Model 623 B | Le Croy | Refer Sr. No 2 of Addresses | |
| 4 Fold Majority Logic Unit | Model 365 AL | Le Croy | Refer Sr. No 2 of Addresses | |
| Fan-In-Fan-Out | Model 428 | Le Croy | Refer Sr. No 2 of Addresses | |
| Dual Programmable Logic Unit | Model C 542 | C.A.E.N | Refer Sr. No 3 of Addresses | |
| High Voltage Power Supply | Model N 126 | C.A.E.N | Refer Sr. No 3 of Addresses | |
| PMT | 9807B | THORN EMI | Refer Sr. No.6 of Addresses | |
| UV Lamp Source/Supply | 6035/6061 | Oriel make | Refer Sr. No.7 of Addresses | |

**Addressses:**

| | **Manufacturer** | | **Local Representative** | |
|---|---|---|---|---|
| 1. | M/S Kinetics Systems Corporation<br>900 N, State Street<br>LOCKPORT, Illinois 60441 | Ph. 815 838 0005<br>Fax 815 838 4423 | M/S Electronic Enterprises<br>M-4/23, Model Town<br>IIIrd Stop DELHI 110009 | Mr. C.P.Sharma<br>Ph. 011 27240436,<br>011 27124915<br>E- Mail: cps-eedel@rediffmail.com |
| 2. | M/ Le Croy<br>700 Chestnut Ridge Road,<br>Chestnut Ridge,<br>NY 10977-6499 USA | Ph. 914 578 6013<br>Fax: 914 578 5984<br>E Mail: Irs_sales @ lecroy.com | As above in Sr. No. 1 | |
| 3. | C.A.E.N<br>COSTRUZIONI APPARECCIATURE ELECTRONISCE NUCLEARI S.p.A<br>Via Vetraia, 11-55049<br>VIAREGGIO (Italy) | Ph. 0584 388398<br>Fax 058 388959<br>E Mail info@caen.it | As Above in Sr. No. 1 | |
| 4. | M/S Phillips Scintific<br>150 Hilltop Road<br>RAMSEY NJ 07446 | Ph. 201 934 8015<br>Fax: 201 934 8269 | M/S CON – SERV-Enterprises<br>B-203 Ani Raj Tower<br>Near GKW, L.B.S.Road<br>Bhandeep (W) Mumbai 400078 | Dr. D.P.Navelkele<br>Ph. 022-5913743<br>E mail: conserve@bom4.vsnl.net.in |
| 5. | M/S Oxford Instruments Inc<br>Nuclear Measurements Group<br>601 Oak Ridge Turnpike<br>Oak Ridge, TENNESEE 37830-756<br>USA | Ph. 423 488 5891<br>Fax: 423 488 5891<br>E Mail nmg@oxfordnm.usa.com | As Above in Sr. No. 1 | |

| | | | | |
|---|---|---|---|---|
| 6. | M/S Thorn EMI Electron Tubes Ltd<br>Bury Street Ruislip<br>Middlesex HA 47TA<br>England | Ph. 0895 630771<br>Fax: 0895 635953 | M/S Parsram & Company<br>206 Keshva, C-5-E,<br>Bandra Kurla Complex,<br>Bandra (E)<br>Mumbai | Ph 022 6407245<br>Fax: 022 6451785 |
| 7. | M/S HAMAMATSU<br>Hamamatsu Photonics KK<br>Solid State Division<br>1126-1, ICHINO-CHO<br>Hamamatsu City 435<br>JAPAN | Ph 053 434 3311<br>Fax 053 434 5184 | | |
| 8. | M/S Oriel Instruments<br>250 Long Beach Boulevard<br>Stratford, CT 06497 0872 | Ph 203 377 8282<br>Fax: 203 378 2457<br>E Mail:<br>73163.1321@compuserve.com | M/S SIMCO Scientific Instruments<br>Marketing Co (P) Ltd<br>SIMCO HOUSE<br>14 Bhawan Kunj<br>Behind Sector D Pocket II<br>Vasant Kunj<br>New Delhi 110070 | Dr. R.S.Daryan MD<br>Ph 011 6890211<br>Fax: 011 6897965 |
| 9. | M/S LEMO S.A<br>Chemin des Champs- Courbes 28<br>P.O. Box 194 Ecublens (Switzerland) | Ph 4121 691 1616<br>Fax: 4121 6911626 | M/S PT Instruments Pvt Ltd<br>6/6/10 Bhawani Nagar<br>P.O.Box No. 17436<br>Andheri (East) Mumbai | Ph 022 851 1353<br>022 852 4605<br>Fax: 022 9122 8501886<br>E Mail:<br>ptind.sameer@gems.vsnl.net.in |